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Long term stability of enhancement mode GaN power devices

Tian-Li WU

Supervisor:
Prof. dr. ir. Guido Groeseneken

Dissertation presented in partial fulfilment of the requirements for the degree of Doctor of Engineering Science (PhD): Electrical Engineering

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KU Leuven
Faculty of Engineering Science
Department of Electrical Engineering
Kasteelpark Arenberg 10, 3001 Leuven, Belgium

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Jury:
Prof. H. Hens, Chair (KU Leuven), Chairman
Prof. G. Groeseneken, Promoter (KU Leuven & imec)
Dr. D. Marcon, Co-promoter & daily supervisor (imec)
Prof. P. Reynaert (KU Leuven)
Prof. J. Driesen (KU Leuven)
Prof. B. Bakeroot (Ghent University & imec)
Prof. M. Meneghini (University of Padova, Italy)
Dr. J. Derluyn (EpiGaN, Belgium)

Tian-Li Wu
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imec

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Uitgegeven in eigen beheer, Tian-Li Wu, Kasteelpark Arenberg 10, B-3001 Leuven (Belgium)

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To my parents

“Once more unto the breach, dear friends, once more!”

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"The Journey is the Reward."

Tian-Li Wu

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Abstract

GaN-on-Si technology (AlGaN/GaN High Electron Mobility Transistors (HEMTs) on Si substrates) shows the promising characteristics and cost-competitiveness of power switching applications. In spite of the extraordinary performance and cost advantages, AlGaN/GaN HEMTs are still limited by their instabilities. For power-switching applications, GaN power devices operate at a high drain voltage during an OFF-state and at a high gate voltage during an ON-state, where good reliability is essential for these operating conditions.

This dissertation focuses on the physical degradation mechanisms in the gate region that play a role in the long-term stability of Au-free enhancement-mode GaN power devices, especially for the two most important architectures: recessed gate Metal-Insulator-Semiconductor (MIS)-HEMTs/-FETs (Field-Effect Transistors) and p-GaN gate AlGaN/GaN HEMTs. Forward gate bias time-dependent dielectric breakdown (TDDB) and positive bias temperature instability (PBTI) are observed in depletion-mode MIS-HEMTs and enhancement-mode MIS-FETs. The percolation model and Weibull distribution are used to understand the degradation mechanisms of forward gate bias TDDB, further calculating the lifetime. Regarding the PBTI, different techniques, i.e. a forward-reverse $I_D V_G$ sweep, a frequency-dependent conductance method, and an AC-transconductance method, are used to characterize the threshold voltage (V_{TH}) hysteresis, interface states density (D_{it}), and the amount of border traps in the devices with different gate dielectrics. Furthermore, an eMSM (extend-Measure-Stress-Measure) method is used to study the stress-recovery phenomena in fully recessed gate MIS-FETs. A physical model, which can nicely reproduce the experimental data, is proposed to explain the origin of PBTI.

Regarding p-GaN gate AlGaN/GaN HEMTs, temperature dependency of the forward bias gate breakdown is observed and characterized. Then, a physical model is proposed to explain the phenomenon. Furthermore, forward gate bias time-dependent p-GaN gate breakdown and positive bias temperature instability (PBTI) are also studied in p-GaN gate AlGaN/GaN HEMTs. The possible mechanisms are proposed to explain the time-dependent p-GaN gate breakdown phenomenon and a negative V_{TH} shift under

a positive gate bias.

Keywords: GaN-on-Si, HEMT, MIS-HEMT, MIS-FET, p-GaN, TDDB, PBTI, Reliability.

Samenvatting

GaN-on-Si-technologie (d.i. AlGaN/GaN Hoge Mobiliteit Transistoren (HEMTs) op Si substraten) toont veelbelovende eigenschappen en goede kostcompetitiviteit voor toepassingen die het schakelen van hoge vermogens vereisen. Ondanks de buitengewone prestaties en kostenvoordelen worden AlGaN / GaN HEMTs nog beperkt door hun instabiliteit. In toepassingen waarbij hoge vermogens moeten geschakeld worden, werken de GaN vermogencomponenten op hoge drainspanning tijdens de UIT-toestand en bij een hoge gatespanning tijdens de AAN-toestand. Daarbij is een goede betrouwbaarheid essentieel.

Dit proefschrift handelt over de degradatiemechanismen in het gebied rond de gate van de transistor, die een rol spelen in de stabiliteit op lange termijn van Au-vrije verrijkings-mode GaN vermogenstransistoren, inzonderheid van de twee belangrijkste architecturen: de Metal-Insulator-Semiconductor HEMT of FET (MIS-HEMT/MISFET) enerzijds, waarbij de AlGaN barriere gedeeltelijk of geheel wordt afgeëtst en de AlGaN/GaN HEMT met p-gedopeerde gate (p-GaN) anderzijds. Tijdsafhankelijke dielectrische doorslag (Time dependent dielectric breakdown of TDDB) onder voorwaartse gatespanning en Positieve Bias TemperatuurInstabiliteit (PBTI) worden waargenomen in MIS-HEMTs, die van het ontruimingstype zijn en MIS-FETs, die van het verrijkingstype zijn. Het percolatiemodel en de Weibull distributie worden gebruikt om de degradatiemechanismen van TDDB onder voorwaartse gatespanning te begrijpen en op deze manier de levensduur te voorspellen. Wat betreft de PBTI worden verschillende technieken gebruikt voor het karakteriseren van de drempelspanning (V_{TH}) hysteresis, en de dichtheid van grensvlaktoestanden (D_{it}) en border traps in de transistoren met verschillende gate dielectrica. De gebruikte technieken zijn o.m. een voorwaartse en achterwaartse I_D-V_G meting, een frequentieafhankelijke conductantiemethode en een AC-transconductantiemethode. Verder wordt een eMSM (extended-Measure-Stress-Measure) methode gebruikt om de stress-herstel verschijnselen in MISFETs met volledig geëtste AlGaN barrière te bestuderen. Er wordt een fysisch model voorgesteld, dat de experimentele gegevens goed kan reproduceren en de oorsprong van PBTI kan verklaren.

In p-GaN gate AlGaN/GaN HEMTs wordt een temperatuursafhankelijkheid van de gate doorslag onder voorwaartse spanning waargenomen en gekarakteriseerd. Vervolgens wordt een fysisch model voorgesteld om het verschijnsel te verklaren. Tenslotte worden ook de tijdsafhankelijke p-GaN gate doorslag onder voorwaartse gatespanning en de PBTI in p-GaN gate AlGaN/GaN HEMTs bestudeerd. Mogelijke mechanismen worden voorgesteld om de tijdsafhankelijke p-GaN doorslag en de negatieve V_{TH} verschuiving onder een positieve gatespanning te verklaren.

Sleutelwoorden: GaN-on-Si, HEMT, MIS-HEMT, MIS-FET, p-GaN, TDDB, PBTI, Reliability.

Abbreviations

Acronym	Description
GaN	Gallium Nitride
AlGaN	Aluminum Gallium Nitride
V_{TH}	Threshold Voltage
LEDs	Light Emitting Devices
AlN	Aluminum Nitride
MBE	Molecular Beam Epitaxy
MOCVD	Metal Organic Chemical Vapor Deposition
HEMT	High Electron Mobility Transistor
WBG	Wide Band Gap
2DEG	Two Dimensional Electron Gas
MIS-HEMTs	Metal-Insulator-Semiconductor High Electron Mobility Transistors
MIS-FETs	Metal-Insulator-Semiconductor Field-Effect Transistors
D-mode	Depletion mode
E-mode	Enhancement mode
GIT	Gate Injection Transistor
RTCVD	Rapid Thermal Chemical Vapor Deposition
ALD	Atomic Layer Deposition
PEALD	Plasma-Enhanced Atomic Layer Deposition
MOS	Metal-Oxide-Semiconductor
TDDB	Time-Dependent Dielectric Breakdown
PBTI	Positive Bias Temperature Instability
NBTI	Negative Bias Temperature Instability
eMSM	Extended-Measure-Stress-Measure
CVS	Constant Voltage Stress
CCS	Constant Current Stress
CMOS	Complementary Metal Oxide Semiconductor
FET	Field Effect Transistor
IL	Interfacial Layer

Acronym	Description
SBD	Soft Breakdown
TEM	Transmission Electron Microscopy
WKB	Wentzel–Kramers–Brillouin (as in ‘WKB approximation’)
EMMI	Emission Microscopy Measurements

List of Symbols

Symbol	Unit	Description
E_G	eV	Bandgap
n_i	cm^{-3}	Intrinsic carrier concentration
n_s	cm^{-3}	Charge density
σ_{2DEG}	-	The total carriers present in the 2DEG
σ_{SURF}	-	The charges present at the AlGaN surface
β	-	Weibull shape parameter or Weibull slope
c_0	m	Lattice constant
C_{13}, C_{33}	Gpa	Elastic constant
ΔE_c	eV	AlGaN/GaN band discontinuity
ϵ_0	F/cm	Dielectric constant in vacuum
e_{31}, e_{33}	C/m^2	Piezoelectric coefficients
E_A	eV	Activation energy
E_{BD}	V/cm	Breakdown field
E_F	eV	Fermi level
Eox	V/cm	Oxide field
ϵ	-	Relative dielectric constant
F(t)	-	Failure distribution function
$F(t_{BD\_i})$	-	Cumulative failure
L_G	μm	Gate lenght
L_{GD}	μm	Gate-drain distance
L_{GS}	μm	Gate-source distance
m	-	Oxide trap generation rate
m*	-	Effective electron mass
n	-	Exponent of the V_G power law model
N_D	cm^{-2}	Donor density
N_{min}	cm^{-2}	Minimum number of traps for oxide breakdown
n_s	cm^{-2}	2DEG carrier density
P_{PZ}	cm^{-2}	Piezoelectric polarization
P_{SP}	cm^{-2}	Spontaneous polarization

Symbol	Unit	Description
q	C	Elementary charge
r	nm	Trap radius on the percolation mode
R_{on}	Ohm/mm	On resistance
σ_{2DEG}	cm^{-2}	2DEG charge density
$\sigma_{AlGaN/GaN}$	cm^{-2}	Polarization charge density at the interface
σ_{POL}	cm^{-2}	Polarization charge density
σ_{SURF}	cm^{-2}	Surface charge density
T	K or °C	Temperature
t_{AlGaN}	nm	AlGaN thickness
t_{BD}	sec	Time-to-breakdown
t_{CR}	nm	Critical AlGaN thickness for 2DEG formation
t_{ox}	nm	Oxide thickness
t_{stress}	sec	Stress time
V_{BD}	V	OFF-state breakdown
V_G	V	Gate voltage
D_{it}	$cm^{-2}eV^{-1}$	Interface state density
D_{ot}	$cm^{-3}eV^{-1}$	Oxide defect density

Contents

Chapter 1

Introduction

The reliability of Gallium Nitride-based devices will be investigated in this thesis. Gallium Nitride (GaN) is a III-V compound semiconductor with extraordinary properties such as a wide band gap and its consequent large breakdown electric field, high thermal stability, and good heat conductivity. In this first chapter, a general overview of GaN-based devices will be provided, including their material properties, device architectures, and reliability issues.

1.1 The birth of GaN-based devices

Although Gallium Nitride (GaN) was first synthesized in 1932 by W.C. Johnson *et al*. [1], it was epitaxially grown on a sapphire substrate only in 1969 by Maurska and Tienjen [2]. This successful demonstration attracted lots of attention regarding GaN-based materials in semiconductor fields, especially for high operating temperature and voltage applications, where wide bandgap materials are highly demanded. Until the last decade of the 20th century, most of the efforts focused on improving the GaN crystal quality and on developing a p-type GaN for light emitting devices (LEDs). Yoshida *et al*. [3] made a breakthrough in showing that GaN crystal quality can be highly improved by using a thin aluminum nitride (AlN) buffer layer, grown between GaN and a foreign sapphire substrate when GaN is grown by molecular beam epitaxy (MBE). Later, Amano *et al.* [4] developed the "two-step method" to grow GaN using metal organic chemical vapor deposition (MOCVD). These two steps include an AlN layer that was first grown at low temperature and a GaN layer that was grown afterward at high temperature. Growing high-quality GaN materials in a MOVCD reactor fits the industrial perspective regarding mass production. The same group also showed that it is possible to obtain p-type GaN via low energy electron beam irradiation (LEEBI) of magnesium (Mg) [5]. As referred to already, these breakthroughs on the epitaxial growth have resulted in a revival of interest within the scientific community in the GaN-based material system. In fact, since the early 1990s, this material has been the subject of intense investigation both for optical and power electronic applications. In 1991, Khan *et al*. [6] observed a spontaneous formation of a two dimensional electron

gas (2DEG) when a thin layer of aluminum gallium nitride (AlGaN) was epitaxially grown on a GaN layer. Two years later, the same group introduced the first High Electron Mobility Transistor (HEMT) based on the AlGaN/GaN material system [7]. On optoelectronics, Nakamura *et al*. [8] demonstrated the first high-brightness blue (HB) double-heterostructure (DH) light emitting diode (LED) (2014 Nobel Prize in physics was awarded to Isamu Akasaki, Hiroshi Amano and Shuji Nakamura for the invention of blue light emitting diodes (LEDs)). Several years later, the same authors also showed the first blue laser based on the GaN material system [9]. At this stage, the performance of GaN-based devices was tremendously improved. Particularly for optical applications, GaN-based devices have reached their technological maturity and are at the stage of commercialization. In contrast, despite enormous progress reported over the last 15 years, GaN-based devices for power electronic applications are yet to reach their maturity. In fact, the GaN-based transistors for RF and power-switching applications available in the market today operate only at a fraction of their potential, which is most probably due to instability. Nevertheless, this fraction of the transistors' total potential is still beyond other available Si- or III-V-based technologies, as will be discussed in the next paragraphs.

1.2 Material properties

1.2.1 Comparison of semiconductor materials

The basic material properties for conventional (Si, GaAs) and Wide Band Gap (WBG) semiconductors are shown in Table 1.1. GaN-based and SiC-based materials have 2-to-3 times larger bandgap (E_G) than those of conventional semiconductors (Si, GaAs), leading to high electric breakdown fields (E_{br} is typically one order of magnitude larger than conventional semiconductors). In addition, the wide bandgap of SiC and GaN results in very low intrinsic carrier concentration (n_i). Therefore, these materials could theoretically have negligible leakage current up to 500°C. This property allows high temperature operation without excessive leakage or thermal runaway, further reducing cooling requirements. However, bulk GaN and SiC have a lower mobility than GaAs. On the other hand, a 2DEG (two dimensional electron gas) can spontaneously be formed at the AlGaN/GaN hetero-junction, allowing for high electron mobility and high saturation velocity. The room temperature mobility of the 2DEG is typically between 1200 and 2000 cm^2/V^1s^1 [10], which is significantly higher compared to the bulk GaN mobility. The 2DEG charge density (n_s) of the AlGaN/GaN structure is very high due to piezoelectric and spontaneous polarization-induced effects [11]. Due to the wide band gap and high electron mobility, AlGaN/GaN high electron mobility transistors (HEMTs) are promising for high-power and high-frequency applications.

Table 1.1: *Comparison of the material properties (Si [12], GaAs [12], 4H-SiC [13], GaN [14] [15], and AlN [14] [15] [16]).*

	Si	GaAs	4H-SiC	GaN	AlN
E_G (eV)	1.1	1.4	3.2	3.4	6.2
ϵ_r	11.7	13.1	10	9	8.5
$\mu_n(cm^2/(V{\cdot}s))$	1500	8500	800	900	300
V_{sat} (10^7cm/s)	1	1	2	2.5	1.4
E_{br} (MV/cm)	0.3	0.4	3	3.3	12
Q (W/(cm·K))	1.5	0.43	3.3	1.3	2
Ni (cm^{-3})	1x10^{10}	1.8x10^{6}	9x10^{-7}	1.9x10^{-10}	9.4x10^{-34}
Nc (cm^{-3})	2.9x10^{19}	4.7x10^{17}	1.6x10^{19}	1.2x10^{18}	6.2x10^{18}
Nv (cm^{-3})	3.1x10^{19}	7x10^{18}	3.19x10^{19}	4.1x10^{19}	4.9x10^{20}

1.2.2 Crystal Structures

GaN-based materials have three different crystal structures, i.e. zincblende, rocksalt, and wurtzite. However, only the wurtzite structure shows thermodynamical stability [17]. The most common growth direction of GaN epitaxial layers is along the c-axis (Figure 1.1). Depending on the different growth conditions, GaN can either have a Ga-face or N-face termination, as schematically shown in Figure 1.1. A different face termination leads to different spontaneous polarization properties due to the charge transfer from the strongly electronegative N and less electronegative Ga. Nowadays, GaN-based devices are normally fabricated with Ga-face termination, which can be easily obtained from a metal organic chemical vapor deposition (MOCVD) reactor. Imec's Au-free CMOS compatible GaN-on-Si technology focuses on the design and fabrication of high performance Ga-face GaN-based devices. Therefore, this thesis will only focus on Ga-face GaN-based devices.

Aluminum nitride (AlN), also of the III-V family, has a wurtzite structure and spontaneous polarization property as well. Therefore, AlN material has also attracted a lot of attention for high power applications. Both GaN and AlN are wide bandgap materials, with bandgap as large as 3.4 eV and 6.2 eV, respectively. This property results in a critical electric field of 3.3 MV/cm for GaN and 12 MV/cm for AlN [16]. On top of that, AlN can form thermal stable alloys with Ga. In particular, by tuning the Al content into an AlGaN layer, it is possible to tune its bandgap: from 6.2 eV of pure AlN (100% Al) to 3.4 eV of pure GaN (0% Al). GaN, AlN, and its alloy AlGaN have different lattice constants, as shown in Figure 1.2. The higher the Al content, the smaller the lattice constant. As will be discussed later, the lattice mismatch between GaN and AlGaN is the origin of piezoelectric polarization when a AlGaN layer is epitaxially grown on top of a GaN material. Spontaneous and piezoelectric polarization properties are the fundamental mechanisms for forming AlGaN/GaN-based electronics.

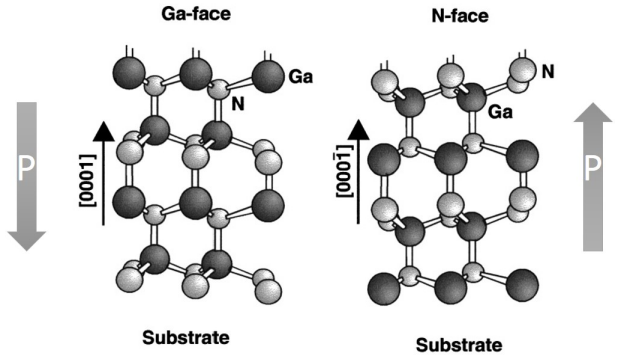

Figure 1.1: *Schematic of the crystal structure of wurtzite Ga-face and N face GaN [17]. The arrow shows the direction of the polarization (P).*

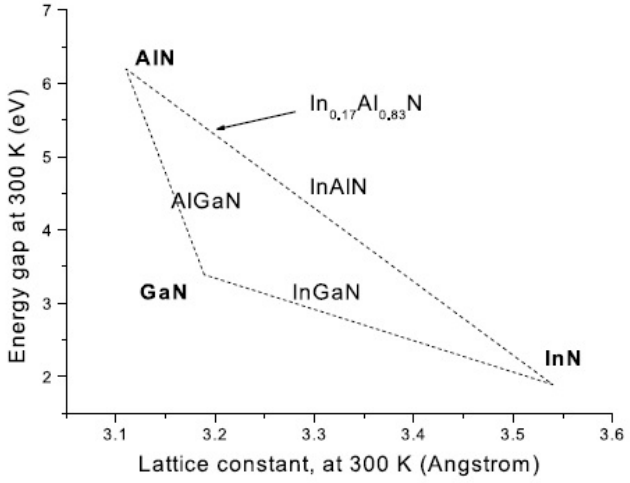

Figure 1.2: *Energy bandgap in relation to the lattice constant of III-nitrides [19].*

Additionally, it is worth mentioning that the chemical bonds of the III-N compound material, such as GaN or AlN, are strong, leading to a very stable material. Moreover, since GaN has the low intrinsic carrier density (10^{-10}cm^3), it becomes a conductor (10^{15}cm^3) when the temperature is above 1300°C. However, Si reaches the same conducting property at only 300°C [18]. This makes GaN intrinsically suitable for high temperature electronic applications as well.

In summary, GaN and AlN are wide bandgap materials with spontaneous polarization

Table 1.2: *Comparison of substrate properties [20]. Note that lattice mismatch and thermal mismatch are calculated by (Substrate-GaN/GaN).*

	Lattice Constant (Å)	Lattice Mismatch (%)	Thermal Expansion Coefficient ($10^{-6}K^{-1}$)	Thermal Mismatch (%)	Thermal Conductivity (W/(cm·K))
GaN	a=3.19	0	5.6	0	1.3
Sapphire	a=4.75	49	7.5	33.9	0.5
SiC	a=3.08	-3.5	4.2	-25	3.3
Si (111)	5.43	70	3.59	-35.8	1.5

properties. They have a maximum breakdown field that is above 3 MV/cm and 12 MV/cm, respectively. This feature, combined with the high temperature stability, makes these materials suitable for high-voltage and high-temperature applications.

1.2.3 Substrates

The GaN epitaxial layer can be grown on different substrates, including GaN, SiC, Sapphire, and Si. GaN-on-GaN would be a perfect choice due to the lattice match. However, the cost and limited size of wafer (2 inch) remain the biggest challenges for mass production. In order to solve these challenges, the GaN epitaxial layer is typically grown on a large-size foreign substrate, such as sapphire (Al_2O_3), silicon carbide (SiC) or silicon (Si), resulting in hetero-epitaxy. However, the thermal and lattice mismatch pose a serious challenge on how to obtain a high quality GaN epitaxial layer (Table 1.2). The dislocation density is typically within a range of 10^7 - 10^9 cm^{-2}.

The GaN-based device was the first to have been demonstrated on a sapphire substrate, which has the advantages of low cost as well as mechanical and thermal stability. Despite still being used in optoelectronics, its low thermal conductivity (Table 1.2) severely limits the power performance of sapphire-based GaN-based power electronic devices. In comparison to sapphire, Si has better thermal conductivity and low cost availability. However, due to the large lattice mismatch (Table 1.2), growing high quality GaN on Si substrates is a big challenge. Nevertheless, by introducing a proper buffer layer and optimizing the growth condition, growing high quality GaN layers on a 8-inch Si substrate [21–24] has recently been demonstrated. This allows for the implementation of the subsequent device processing in an already existing Si-based processing environment, offering advances in terms of cost, reliable device processing, and high throughput. Without a doubt, SiC is the best substrate to grow GaN (Table 1.2). Due to the small lattice mismatch between SiC and GaN, high quality GaN films can be

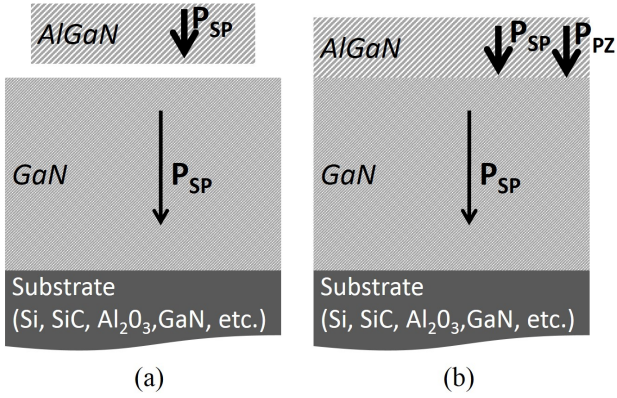

Figure 1.3: *Schematic of an AlGaN/GaN heterostructure. On top of a thick GaN layer, a thin layer of AlGaN is epitaxially grown. Due to the lattice mismatch between GaN and AlGaN (a thin AlGaN layer is shown in (a)), a piezoelectric component (P_{PZ}) is added to the spontaneous polarization (P_{SP}), as shown in (b). Since the GaN layer is relaxed, only the spontaneous polarization (P_{SP}) is present in this layer.*

grown on SiC without introducing several buffer layers, as in the case on Si. In addition, the excellent thermal conductivity on SiC (Table 1.2) allows for proper heat dissipation when the GaN-based devices are under high power operation. Unfortunately, the SiC substrate (>2000 Euro) is more expensive than Si (111) substrate. Consequently, this has a considerable impact on the device cost, further limiting the use of GaN-based technology grown on a SiC substrate.

1.2.4 AlGaN/GaN heterostructure and two dimensional electron gas (2DEG)

One of the most attractive points in GaN-based devices for power switching applications is the natural existence of a two dimensional electron gas (2DEG) in the AlGaN/GaN heterostructure. An AlGaN/GaN heterostructure can be formed by epitaxially growing a thin AlGaN layer on top of a thick GaN layer, as depicted in Figure 1.3. Therefore, due to the spontaneous and piezoelectric polarization, a two dimensional electron gas (2DEG) is subsequently formed at the interface between the AlGaN barrier and the GaN channel, the details of which will be described in the following.

GaN and AlN both present a strong spontaneous polarization (P_{SP}) since N atoms are strongly electronegative and Ga or Al atoms are less electronegative. Table 1.3 shows

Table 1.3: *Lattice constant, relative dielectric constants, spontaneous (P_{SP}), piezoelectric coefficients (e_{33} and e_{31}) and elastic deformation constants (C_{13} and C_{33}) for AlN, GaN and AlGaN in function of x = Al% content [17].*

	AlN	GaN	$Al_xGa_{1-x}N$
Lattice constant (Å)	3.11	3.19	-0.08x+3.19
Relative dielectric const.	9	9.5	-0.5x+9.5
$P_{SP}(C/m^2)$	-0.081	-0.029	-0.052x-0.029
$e_{33}(C/m^2)$	5.43	70	0.73x+0.73
$e_{31}(C/m^2)$	-0.60	-0.49	-0.11x-0.49
C_{13}(Gpa)	108	103	5x+103
C_{33}(Gpa)	373	405	-32x+405

the spontaneous polarization coefficients. The strong spontaneous polarization present in these materials leads to the high spontaneous polarization coefficients reported in Table 1.3.

A piezoelectric polarization (P_{PZ}) component appears on GaN, AlN or AlGaN when the material is strained. By using the parameters in Table 1.3, it is possible to directly calculate this component for a strain along the a-axis (Figure 1.1) as follows [17]:

$$P_{\mathrm{PZ}} = 2\frac{a - a_0}{a_0}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) \tag{1.1}$$

where the first component (a - a_0 / a_0) represents the in-plane strain, i.e. a_0 is the intrinsic lattice constant of the material and a is the resulted lattice constant induced by the applied strain.

In the AlGaN/GaN heterostructure, the piezoelectric polarization appears only in the AlGaN layer since it is under tensile strain; however the GaN layer is normally relaxed. Therefore, the piezoelectric polarization component is calculated for an $Al_xGa_{1-x}N$ layer when grown on top of a GaN layer. In this case, since the AlGaN layer is under tensile strain, the piezoelectric and spontaneous polarizations are parallel (Figure 1.3). So, the piezoelectric and spontaneous polarizations have to be summed up [25].

The explicit calculation of the piezoelectric and spontaneous polarization present in a generic $Al_xGa_{1-x}N$ layer when grown on top of a GaN layer is reported in Figure 1.4. From this figure, it is possible to observe that the higher the Al content, the larger the piezoelectric polarization component, which is caused by a larger lattice mismatch with the GaN layer (Figure 1.4).

Consequently, the higher the Al content in the AlGaN layer, the larger the total polarization. A polarization charge density (ρ_p) is associated with a gradient of

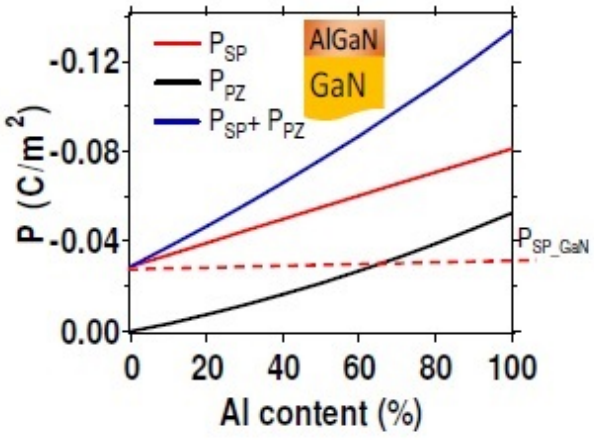

Figure 1.4: *Spontaneous (P_{SP}) and piezoelectric (P_{PZ}) polarization vs. Al content. Since the AlGaN is under tensile strain, the two polarizations can be added [26].*

polarization (P) in space ($\rho_P = \nabla P$). Therefore, at the abrupt interface AlGaN/GaN, a fixed polarization charge should be induced. Considering the case of a tensile strain $Al_xGa_{1-x}N$ layer grown on top of a GaN buffer (Figure 1.3), a fixed positive induced polarization charge appears at the interface of these materials (Figure 1.5) due to the abrupt gradient in polarization between GaN and the tensile strain AlGaN layer. The polarization induced charges scale with the Al content of the AlGaN layer (Figure 1.5) since a higher Al content induces a larger polarization gradient at the interface.

The positive polarization-induced charges at the interface of AlGaN/GaN attract free electrons, resulting in the spontaneous formation of a two dimensional electron gas (2DEG) [17] at the AlGaN/GaN interface (Figure 1.6).

Although the polarization charges at the interface are fixed, the electrons of the 2DEG are free to move. In addition, due to the band discontinuity between AlGaN and GaN, electrons on the 2DEG are well confined into a quantum well, as schematically shown in Figure 1.6(b).

The positive polarization-induced charges at the AlGaN/GaN interface might be responsible for the tendency of electrons to be collected at the heterointerface. However, Ibbetson *et al*. [27] have pointed out that these polarization charges could not be the source of electrons. Several considerations can be made in order to elucidate the origin of the 2DEG [27] with regard to the general AlGaN/GaN heterostructure. First, in the absence of an external applied field, the heterostructure must be neutrally charged. This indicates that all the charges present in the structure must be compensated. So, the

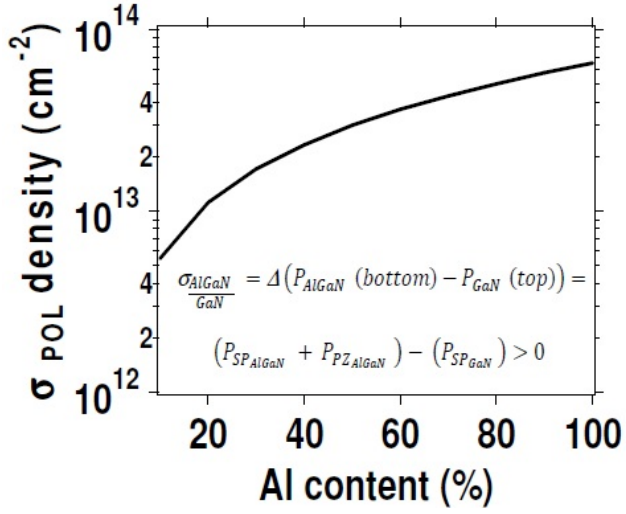

Figure 1.5: *Polarization-induced charges at the interface AlGaN/GaN as a function of the Al content in an AlGaN layer [26].*

contribution of the polarization-induced charges, caused by their dipoles to the total space charge, is exactly zero. The second point is that the 2DEG cannot be generated thermally from the GaN buffer since the buffer charges must be negative, otherwise the electrons in the 2DEG would not be confined at the interface. Moreover, considering a well-designed epitaxial layer, the buffer charges should be as small as possible. So, they can be neglected. Therefore, by setting the buffer charges at zero and by canceling the contribution of spontaneous, piezoelectric, and polarization-induced charges (since they are dipoles), it is possible to obtain the following charge balance equation that indicates the vertical neutrality (Figure 1.6 (a) and (c)):

$$\sigma_{\mathrm{SURF}} + \sigma_{\mathrm{2DEG}} = 0 \tag{1.2}$$

where it is assumed that a truly undoped AlGaN barrier layer is used. Otherwise, a contribution from the ionized AlGaN doped charges must be taken into account.

Equation 1.2 clearly states that the total carriers present in the 2DEG (σ_{2DEG}) must be equal to the number of positive charges present at the AlGaN surface (σ_{SURF}), as shown in Figure 1.6 (a) and (b). Therefore, this suggests that the source of electrons can be found in ionized donor-like states present at the AlGaN surface. Consequently, the formation of 2DEG is most probably due to donor-like surface states at the AlGaN

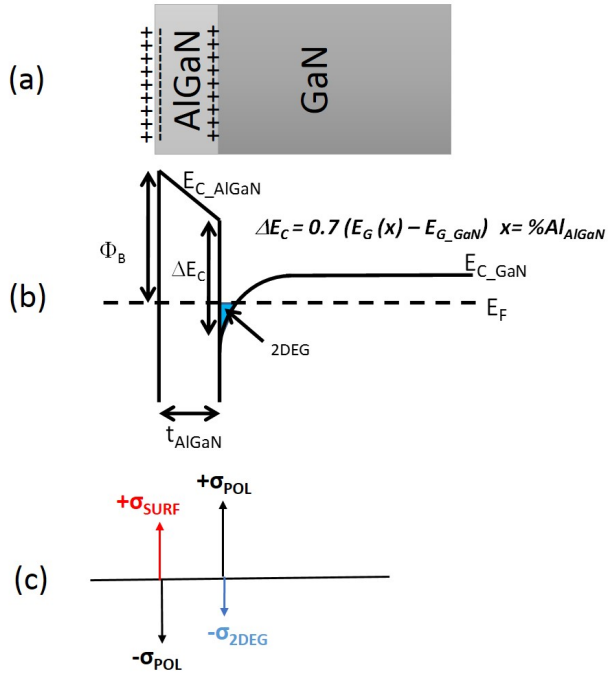

Figure 1.6: *Schematic of the charge distribution and band diagram of the AlGaN/GaN heterostructure. Schematic of the AlGaN/GaN epilayer stack together with the induced charges at the AlGaN surface and AlGaN/GaN interface (a) as well as the band diagram of the AlGaN/GaN heterostructure (b). Note that the band discontinuity between AlGaN and GaN results in a formation of the quantum well where the two dimensional electron gas (2DEG) is confined (b). Therefore, the magnitude and sign of the charges present in the structure are schematically illustrated (c).*

surface. This is called the surface donor model. Note that recent publications [28] [29] have revisited this model with taking into account buffer charges, interface charges, and bulk gate dielectric charges, while the basic concept remains the same.

The surface donor model explains the experimental observation that the 2DEG can be formed only beyond a critical AlGaN barrier thickness. For example, as shown in Figure 1.7 of the device with $Al_{0.34}Ga_{0.64}N$ barrier, the 2DEG density approaches zero when the barrier thickness is below ~ 30 Å. It considers the specific example of an undoped barrier ($\sigma_{\mathrm{AlGaN}} = 0$) with a surface state at an energy E_D below the conduction band edge while assuming that this state is donor-like, i.e. neutral when occupied, positive when empty. Therefore, n_S depends on occupancy of the surface donor state (σ_{SURF})

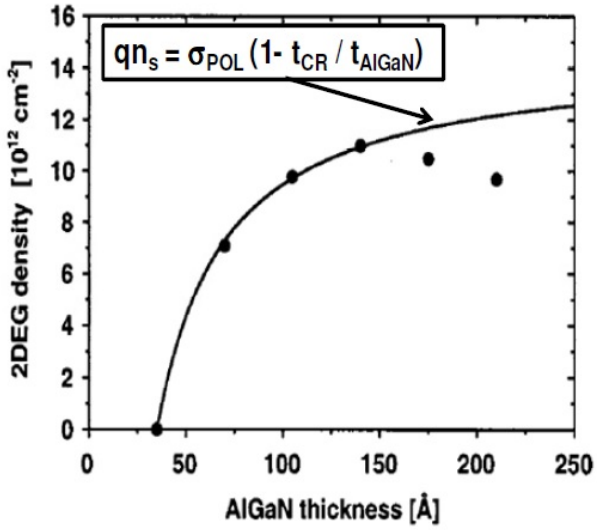

Figure 1.7: *The room temperature 2DEG density when measured as a function of $Al_{0.34}Ga_{0.64}N$ barrier thickness. The curve is the least square fitted to 15 nm data of the surface donor model's equation (inset) [27].*

and its energy relative to the Fermi level, E_F. If the state is sufficiently deep (below E_F), there is no 2DEG since σ_{SURF}=n_S=0 (Figure 1.8). However, since there is a constant electric field in the AlGaN barrier due to the unscreened polarization dipole, E_F-E_D decreases as barrier thickness increases. Beyond the critical thickness of the AlGaN barrier, the donor energy can also reach the Fermi level. Partially-unfilled surface donors become a positive surface charge. Then, 2DEG is created in order to maintain the charge neutrality (Figure 1.8(b)) [27].

Furthermore, it is also possible to analytically calculate the critical barrier thickness at which the 2DEG starts forming, as laid out in the following [27]:

$$t_{\mathrm{CR}} = \varepsilon \frac{E_{\mathrm{D}} - \Delta E_{\mathrm{C}}}{q\sigma_{\mathrm{POL}}} \tag{1.3}$$

where ε is the AlGaN relative dielectric constant (Table 1.3), σ_{POL} is the polarization induced charge at the AlGaN/GaN interface (Figure 1.7), ΔE_{C} is the AlGaN/GaN band discontinuity (Figure 1.6), and E_{D} is the energy level of the surface donors (Figure 1.8).

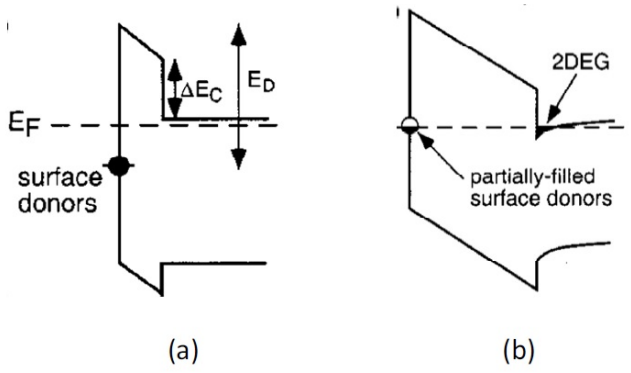

Figure 1.8: *Schematic band diagram of the surface donor model with the undoped AlGaN barrier thickness (a) less than, and (b) greater than, the critical thickness of the 2DEG's formation [27].*

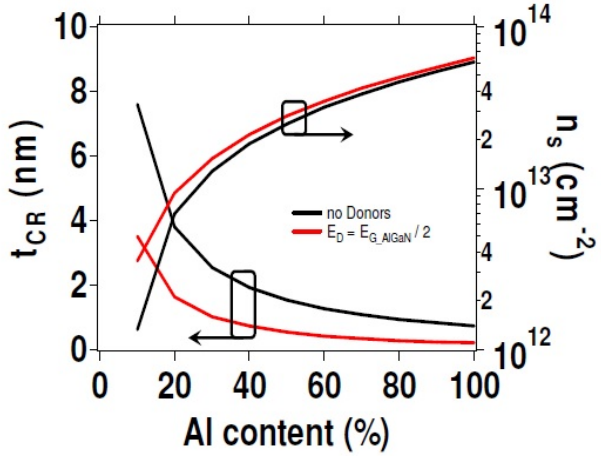

Figure 1.9: *The minimum AlGaN thickness (t_{CR}) (left scale) that allows for the formation of the 2DEG at the AlGaN/GaN interface in function of the Al content present in the AlGaN for two different surface configurations (with and without surface donors). The resulting 2DEG density (right scale) for the 10-nm-thick AlGaN layer is calculated by means of the surface donor model [27] in function of the Al contents [26].*

From equation 1.3, the larger the polarization-induced charge density (σ_{POL}), the smaller the critical barrier thickness for the 2DEG formation that could be obtained (Figure 1.9).

Eventually, when t_{AlGaN} is larger than t_{CR}, it is also possible to calculate the 2DEG carrier density (n_s) based on the surface donor model [27], as follows:

$$qn_s = \sigma_{POL}(1 - \frac{t_{CR}}{t_{AlGaN}}) \tag{1.4}$$

where t_{AlGaN} is the AlGaN thickness as indicated in Figure 1.6.

From Figure 1.7, this model correctly predicts that the 2DEG density will rapidly increase once the critical barrier thickness is exceeded before the 2DEG gradually saturates at σ_{POL}/q for t » t_{CR}.

Furthermore, the model introduced by [27] can be extended to the ideal case of an AlGaN surface where the only available occupied states are in the valence band (no surface states) (Figure 1.9). In this case, the 2DEG can exist once the AlGaN barrier is thick enough for the valence band to reach the Fermi level at the surface. Then, electrons can be transferred from the AlGaN valence band to the GaN conduction band, leaving behind a surface hole gas. The solution of the Poisson equation for this case is similar to the surface donor case, except that the critical thickness is determined by E_{GAlGaN}, i.e. the AlGaN band gap, instead of E_D in equation 1.3.

Figure 1.9 shows the minimum critical thickness and resulting 2DEG in the ideal case of no surface donors, as well as the case of surface donors located in the middle of the AlGaN band gap.

From the whole discussion above, it is clear that the 2DEG density is strongly influenced by the thickness and Al content of the AlGaN barrier. Ideally, growing a thicker AlGaN barrier with a higher Al content leads to higher 2DEG density, e.g. the extreme case of pure AlN. This would also result in a larger bandgap discontinuity at the interface, further providing a better carrier confinement.

Unfortunately, the AlGaN barrier layer starts to relax by cracking when the AlGaN barrier is beyond the critical thickness [30]; this phenomenon lowers the piezoelectric components and consequently reduces the 2DEG concentration.

Furthermore, this critical thickness is a function of the Al content: the higher the Al content, the lower the critical thickness (Figure 1.10). This means that a tradeoff between the Al content and final thickness of the AlGaN barrier layer needs to be taken into account.

Typically, the Al content and thickness of AlGaN barrier layers are typically found within a range of 15 to 35% and 10 to 30 nm, respectively. Nevertheless, this still results in a very large 2DEG density (close to 1×10^{13} cm^{-2}), as calculated before (Figure 1.9). Such a high carrier density is also routinely measured in imec's AlGaN/GaN epilayers, confirming experimentally the predicted values from the surface donor model.

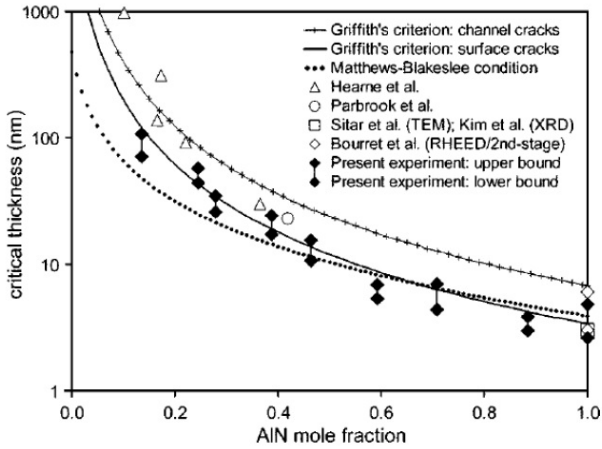

Figure 1.10: *Comparison of measured (data points) and calculated (lines) critical thicknesses for strain relaxation in the $Al_xGa_{1-x}N$/GaN heterostructure [31].*

1.3 Device architectures and processes

1.3.1 AlGaN/GaN High Electron Mobility Transistors (HEMTs)

The spontaneous formation of a sheet of free-moving electrons (2DEG) when a thin layer of AlGaN is epitaxially grown on top of a GaN layer has been extensively discussed in the previous sections. Due to the high carrier concentration and the high mobility guaranteed by the unintentional doped structure, the 2DEG works as an ideal transistor channel. Therefore, an AlGaN/GaN High Electron Mobility Transistor (HEMT) was first demonstrated in [7], where the 2DEG is present at the interface between the AlGaN and GaN buffer. AlGaN/GaN HEMT is a three-terminal device, which has a Schottky metal gate and an Ohmic contact on the drain and source electrode. The current between source and drain contact can flow through the two dimensional conducting channel (Figure 1.11 (a)). The channel is controlled by applying a gate voltage that can locally deplete it, thereby interrupting the conduction (Figure 1.11 (b)). Later on, more and more groups [11] [32] [33] have reported high performance AlGaN/GaN HEMTs for RF as well as for high power applications. It is worth noting that AlGaN/GaN shows a depletion-mode characteristic, which has a negative V_{TH} (V_{TH}<0) and thus needs a negative gate bias to deplete the channel.

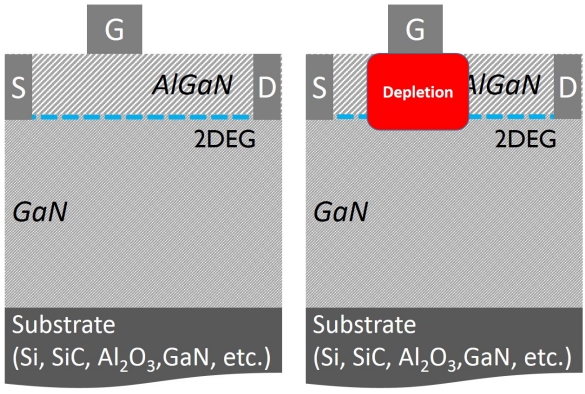

Figure 1.11: *Schematic drawing of an AlGaN/GaN HEMT and its working principle under (a) ON-state and (b) OFF-state condition.*

1.3.2 AlGaN/GaN Metal-Insulator-Semiconductor High Electron Mobility Transistors (MIS-HEMTs)

Conventionally, the Schottky gate AlGaN/GaN HEMTs (Figure 1.12 (a)) suffer from high gate leakage currents under both ON-state and OFF-state conditions due to the typical Schottky gate leakage current and the surface charge current by the surface defect charge [34–37]. Therefore, high forward gate leakage current limits the possibility to apply a high gate voltage in AlGaN/GaN HEMTs. Considering the DC power consumption, it is necessary to reduce the gate leakage current under the OFF-state. For power switching applications, AlGaN/GaN HEMTs need to have a gate bias swing as large as possible (e.g. more than 5V of the gate bias swing in silicon-based power devices) in order to switch quickly from an OFF-state (a large drain bias and a negative reverse gate bias) to an ON-state (a large forward gate bias).

To achieve such a low leakage current, inserting a gate dielectric between the gate metal and AlGaN barrier can efficiently suppress the gate leakage issue, which is normally called AlGaN/GaN Metal-Insulator-Semiconductor High Electron Mobility Transistors (MIS-HEMTs) (Figure 1.12 (b)). AlGaN/GaN MIS-HEMTs have been demonstrated with different gate dielectrics, such as MOCVD grown *in-situ* SiN [38] [39], LPCVD SiN [40], Al_2O_3 [41], HfO_2 [42], etc.

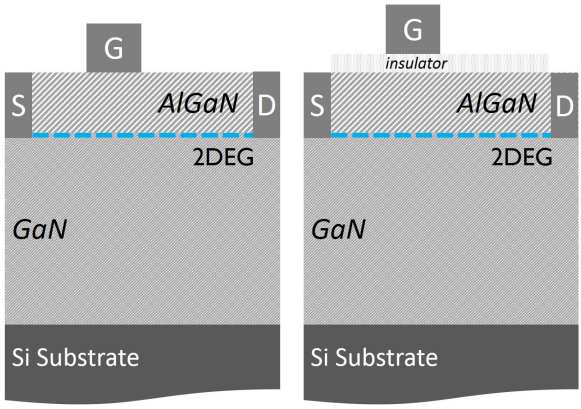

Figure 1.12: *Schematic of a Schottky gate AlGaN/GaN HEMT(a) and a AlGaN/GaN MIS-HEMT(b).*

1.3.3 E-mode AlGaN/GaN-based technologies

The natural form of GaN-based devices is a normally-on or depletion mode (D-mode) device, as mentioned before. Although these type of devices can be used in power semiconductor systems by means of special gate drivers or in a cascode package solution, the market demands for normally-off or enhancement mode (E-mode) devices due to a practical consideration to avoid the failure of the gate drivers, which could destroy the entire system when the device cannot be switched off. So far, there have been several approaches to realize an enhancement mode operation; these include a recessed gate structure [23, 43–46], p-GaN gate [47–50], p-AlGaN gate [51], fluoride-based plasma treatment [52], the piezoneutralization layer [53], floating charges [54], the metal–oxide–semiconductor field-effect transistor structure [55] [56], etc. (Figure 1.13 [57]).

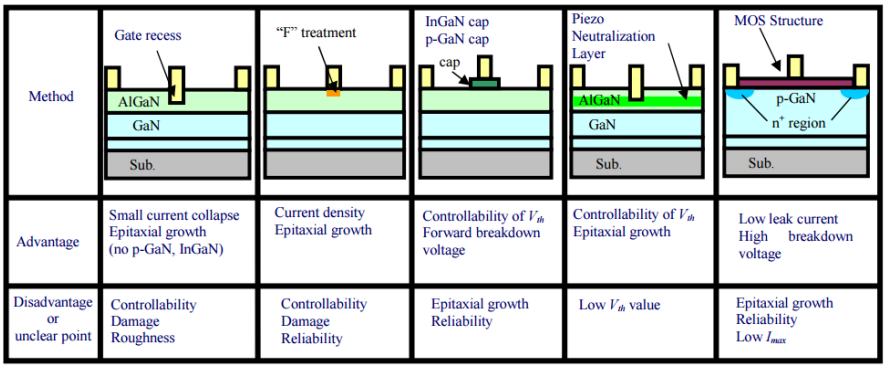

Figure 1.13: *The approaches to realize enhancement mode GaN device [57].*

E-mode GaN MIS-FETs with recessed gate process

A recessed gate technique is considered the most straightforward approach to obtain an enhancement mode characteristic. The 2DEG under the gate is reduced once the AlGaN barrier is below a critical thickness (Figure 1.9), which can "easily" be realized by a well-controlled etching process. In order to gain a sufficient high V_{TH}, a completely gate recessed etching through the AlGaN barrier (even deep into the GaN channel) (Figure 1.14) is preferred [23] [58] although the ON-resistance (R_{on}) could increase due to the reduction of 2DEG under the gate. Gate recessed approaches are generally combined with a gate dielectric deposition in the gate recessed area to suppress the gate leakage issue. Unlike the MIS-HEMTs, where the gate dielectric is on top of the AlGaN barrier (Figure 1.12 (b)), such kind of device structure is typically referred to as GaN Metal-Insulator-Semiconductor Field-Effect-Transistors (MIS-FETs).

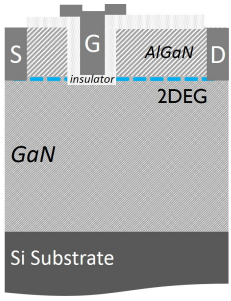

Figure 1.14: *Schematic of fully recessed gate GaN MIS-FET.*

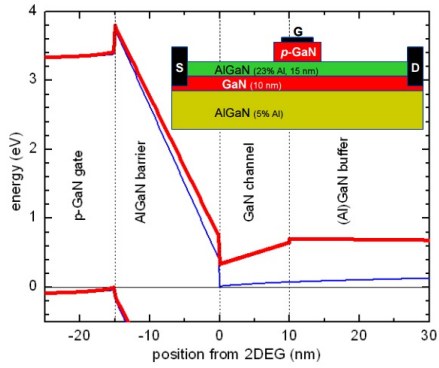

Figure 1.15: *Simulated band structure at the gate position for a device with GaN buffer (thin, blue) and a device with $Al_{0.05}Ga_{0.95}N$ buffer (bold, red). Schematic cross section of the p-GaN gate GaN transistor (inset) [47].*

E-mode p-GaN gate AlGaN/GaN HEMTs

The p-GaN gate AlGaN/GaN HEMT was first demonstrated by Hu *et al.* [59] to be capable of achieving an enhancement mode characteristic. Afterwards, more and more research groups [47, 49, 50, 60] also reported E-mode p-GaN gate HEMTs. Figure 1.15 shows a typical p-GaN AlGaN/GaN HEMTs. The p-GaN gate is able to lift the potential well of the transistor channel (the interface between AlGaN and GaN) out of the Fermi level, resulting in an enhancement mode characteristic. Please note that not only a Ohmic gate metal [47] but also a Schottky gate metal [60] on top of p-GaN barrier is able to realize an E-mode characteristic. Although both architectures lead to an E-mode characteristic, the device with a Schottky gate metal has been demonstrated with a low gate leakage current [60]. However, the detailed study on the device phyics is lacking and worth an in-depth research.

Not only the p-GaN gate but also the p-AlGaN gate (on top of the AlGaN barrier) is able to lift up the Fermi level. Uemoto *et al.* [51] demonstrated the p-AlGaN gate AlGaN/GaN HEMT, which is also called the gate injection transistor (GIT), as shown in Figure 1.16.

Other E-mode technologies

Several other E-mode technologies, e.g. fluoride-based plasma treatment [61], the piezoneutralization layer [53], the metal–oxide–semiconductor field-effect transistor structure [55] [56], floating charges [54], etc., have been proposed. The fluorine ions

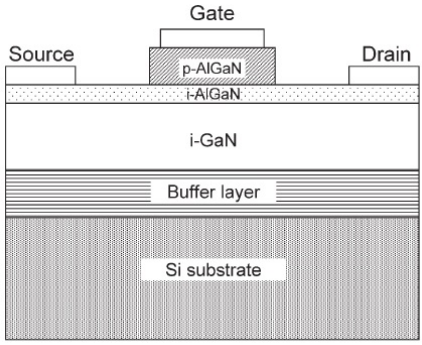

Figure 1.16: *Schematic illustration of the p-AlGaN gate AlGaN/GaN HEMTs [51].*

are able to introduce acceptor-like negative charges deep into the AlGaN barrier, further lifting up the band diagram to realize an E-mode characteristic. However. the instability of these negative charges results in a V_{TH} shift. MIS-HEMTs with a piezoneutralization layer can achieve an enhancement characteristic without being fully gate recessed [53]. However, this concept has not widely been applied into the GaN community, which is most probably due to the complicated design and control of the Al content in the AlGaN barrier and the difficulty of achieving a high V_{TH}. The metal–oxide–semiconductor field-effect transistor structure [55] [56] shows a high V_{TH} and high breakdown voltage. However, the low I_{DS} (due to the low inversion channel mobility) limits the the device's performance. The floating charges [54] concept can achieve a high V_{TH}. However, the injected electrons into the gate dielectric are not stable at a high temperature, further exacerbating the instability of V_{TH}.

1.3.4 Imec's Au-free CMOS-compatible E-mode technologies

At imec, there are two main tracks for E-mode technologies: 1) recessed gate MIS-FETs and 2) p-GaN gate HEMTs. The main steps for the device fabrication are shown in Figure 1.17. A schematic of these devices and a brief description are shown in the following.

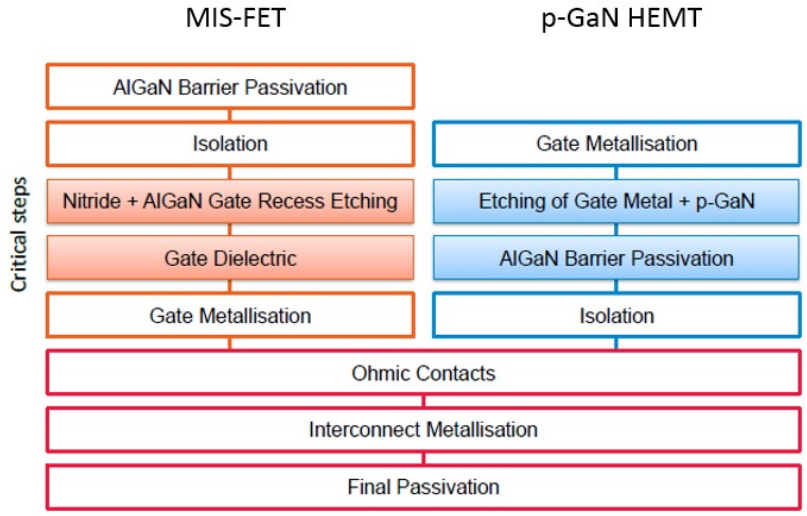

Figure 1.17: *Process flow for a recessed gate MIS-FET and p-GaN HEMT [62].*

E-mode recessed gate MIS-FETs

As mentioned before (Figure 1.14), recessing in the gate region is able to reduce the 2DEG under the gate region, further leading to an E-mode characteristic. One of imec's E-mode technologies is to focus on the development of low damage and well-controlled recessed etching as well as low interface state density and high quality gate dielectric deposition for recessed gate MIS-FETs. A schematic of this device is shown in Figure 1.18. The different gate dielectrics, including RTCVD (Rapid Thermal Chemical Vapor Deposition) SiN, ALD (Atomic layer deposition) Al_2O_3, and PEALD (Plasma-Enhanced Atomic Layer Deposition) SiN, are deposited to compare the transistor's performance and reliability.

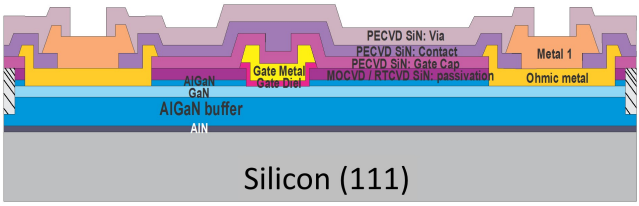

Figure 1.18: *Schematic of E-mode recessed gate MIS-FETs.*

E-mode p-GaN gate AlGaN/GaN HEMTs

The other main track at imec to develop an E-mode GaN-based power device is to focus on p-GaN gate AlGaN/GaN HEMTs. Two different gate metals, i.e. Ohmic metal gate [47] [49] and Schottky metal gate [60] have been used in p-GaN HEMTs. In order to develop low gate leakage current devices, imec focuses on the development of p-GaN gate HEMTs with a Schottky gate metal. A schematic of the device is shown in Figure 1.19.

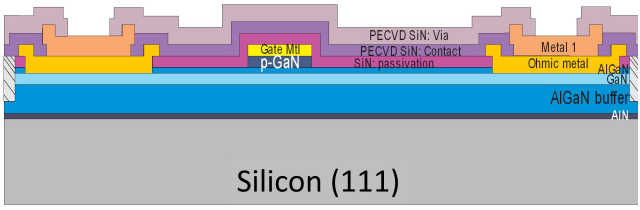

Figure 1.19: *Schematic of E-mode p-GaN AlGaN/GaN HEMTs.*

1.4 Overview of reliability issues in GaN power devices

1.4.1 Introduction

A comprehensive understanding of degradation mechanisms and the related detrimental effects on GaN-based transistors is essential for the design of more effective devices as well as for improving their robustness under operation conditions. Therefore, GaN-based devices need to be examined using various reliability tests in order to verify their capabilities for power switching applications. As schematically shown in Figure 1.20, a power device continuously switches from an OFF-state to an ON-state condition. Therefore, the stability of GaN-based devices needs to be tested in regions, such as ON-state, OFF-state, and SEMI-ON state. In this chapter, we will give a detailed review of reliability-related issues in GaN-based power switching devices.

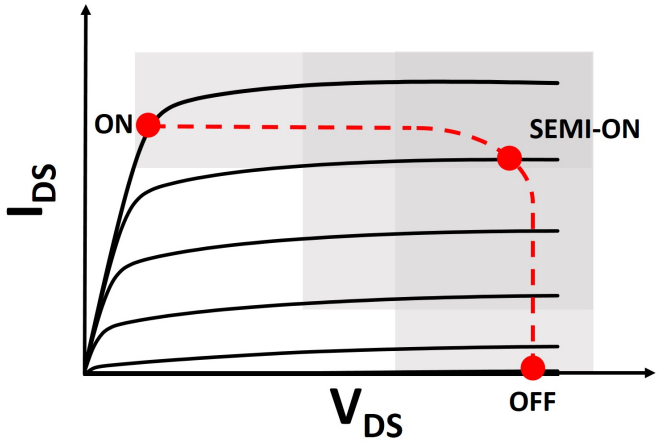

Figure 1.20: *Schematic of I_D–V_D curve of a hard-switching transition between ON/OFF state with an inductive load.*

1.4.2 OFF-state related reliability issues

Under an OFF-state condition, the device is biased at a high drain voltage under the cut-off condition, as shown in Figure 1.20. Due to a high electric field on the drain

side, such bias condition could induce various instabilities, such as current degradation, high leakage current, and gate degradation.

Current degradation after a high voltage OFF-state, i.e. Current Collapse or Dynamic R_{ON}

The most well-known stability issue under OFF-state condition is current degradation, which is typically called current collapse in the GaN community, as shown in Figure 1.21. When the device is switched from an OFF-state (at a high drain bias) to an ON-State (at a low drain bias), the ON-resistance increases. The increase of the ON-resistance can gradually recover. This phenomenon is attributed to trapping issues at the surface [63] or in the buffer [64]. Such current degradation was first discovered in RF GaN-based devices and highly limits the output-power density [65]. In power switching applications, this phenomenon is also refereed to as dynamic R_{ON} [66]. A critical requirement for high efficient power electronics is to keep a low ON resistance (R_{ON}) when switching from a high-voltage OFF state, e.g. V_{DS}>200V, to a low-voltage ON state. This issue leads to an increase in the dynamic ON resistance after an OFF-to-ON switching event. R_{ON} can remain high from nanoseconds (ideal case) to milliseconds or even longer [67].

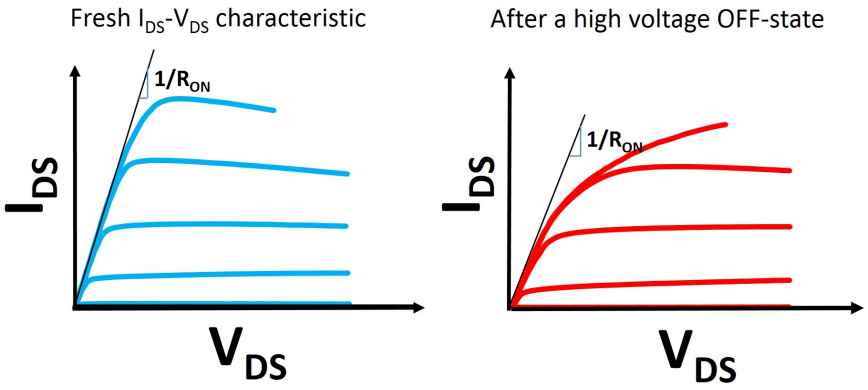

Figure 1.21: *Current degradation (dynamic R_{ON}) in AlGaN/GaN transistors after a high voltage OFF-state.*

Vetury *et al.* [63] have proposed a 'virtual gate' model to explain such current degradation. This degradation mechanism can be explained as follows: during a negative gate bias, electrons flowing from the gate electrode are captured by the empty surface states at the area between the gate and drain, as shown in Figure 1.22. These

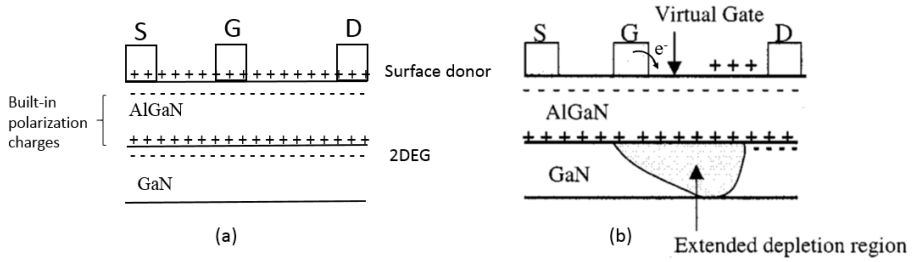

Figure 1.22: *Schematic of the charge distributions in the fresh device (a) and model of the device showing the location of the virtual gate (b) [63].*

electrons, trapped by the surface states, result in a virtual gate due to the reduction in the amount of net positive charges at the surface in donor-like states, leading to a decrease in the drain-source current and transconductance.

There are two mechanisms that allow electrons to be trapped by the surface charge: 1) Electrons could tunnel from the gate into the surface states [63] [68] [69]. 2) Under a high drain voltage, hot electrons in the channel could overcome the potential barrier of the AlGaN barrier, further trapping them at the surface [70] [71].

It is worth mentioning that, under a high electric field, bulk traps can also be one of the dominant aspects for the current collapse, which is typically called buffer-related current collapse [64]. Buffer-related current collapse is most probably due to electron injection into the buffer followed by trapping at deep levels. These deep levels are a necessary requirement for device operation since they suppress buffer leakage and short channel effects [72]. The GaN buffer originally provided the insulating property, further leading to outstanding device performance [72]. Recently, AlGaN/GaN HEMT devices have often preferred to use extrinsic deep-level dopants to improve the buffer's insulating properties, which is partly due to the convenience of monitoring and better control during growth. The two widely used buffer dopants are iron (Fe) and carbon (C). The electrons can be trapped by these extrinsic deep-level dopants, leading buffer-related current collapse. The concept of virtual gate can also be applied to explain the trapping phenomena by the GaN-buffer layer, as shown in Figure 1.23. Note that it is shown in [73] and again in [64] that the distribution and density of dopants have a strong impact on current collapse. Furthermore, the buffers with optimized layers [74] and the distribution and density of dopants [75] can improve this issues.

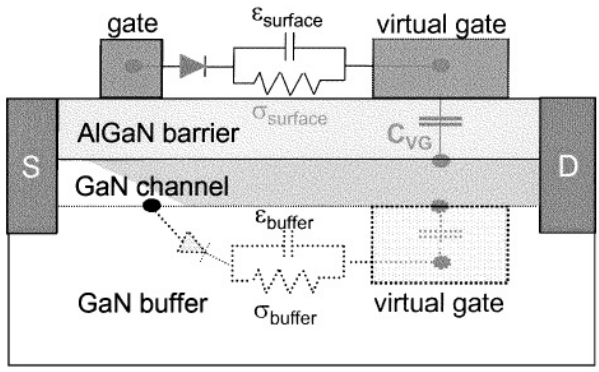

Figure 1.23: *Schematic of the surface and bulk virtual gate concept, showing the trapping phenomena at the surface or GaN buffer, respectively [68].*

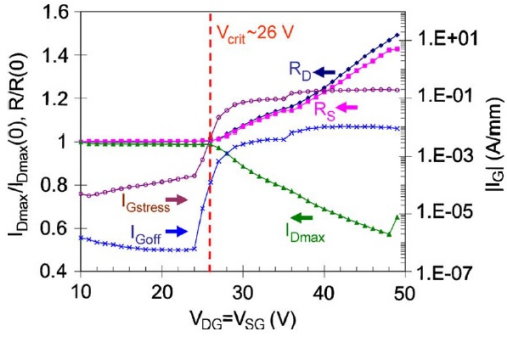

Figure 1.24: *The change in normalized I_{Dmax}, R_D, R_S, $I_{Gstress}$, and I_{Goff} as a function of stress voltage in a step-stress experiment under V_{DS} = 0 (V_{DG} = 10−50 V in 1-V steps) [76].*

OFF-state time-dependent gate edge degradation

When a high reverse bias voltage is applied to the gate (with V_S=V_D=0V), degradation in electrical characteristics, including an increase in gate leakage, current degradation, an increase in drain and source parasitic resistance, and a decrease in DC saturation current I_{DSS}, has been observed [76–79]. Figure 1.24 shows an example of such degradation under a high reverse bias voltage. This is mainly due to the generation of defects at the gate edges, where the electric field is higher. A typical simulated example is shown in Figure 1.25.

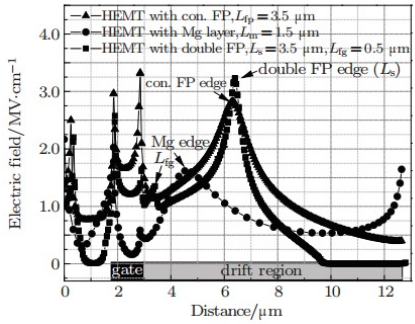

Figure 1.25: *Simulated surface electric distributions along the AlGaN/GaN interface for a HEMT at V_{GS}=-5V [80].*

By using a reverse gate bias step-stress experiment, Meneghesso *et al.* [81] illustrated the creation of localized damage, inducing several sudden "jumps" in the leakage current, with each "jump" corresponding to the creation of a new breakdown point. This leads to a very noisy leakage current. Such features are similar to the phenomenon of time-dependent dielectric breakdown in conventional metal-oxide-semiconductor (MOS) transistors, as shown in Figure 1.26.

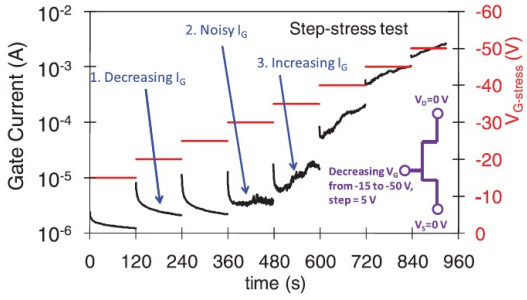

Figure 1.26: *(Color online) During stress (for $|V_G|$<30 V), the gate current decreases monotonically during each step. At a certain step (for V_G=-30 V), gate current becomes noisy, indicating that the device is about to degrade. Degradation is detected as a non-recoverable increase in gate current (see step at V_G=-35V and beyond). Inset: schematic representation of the adopted stress conditions [82].*

Marcon *et al.* [79] found that gate degradation occurs under a low gate voltage, which has a strong voltage-accelerated kinetics and weak-temperature dependence. Marcon *et al.* [79] also showed the time dependency of gate degradation (Figure 1.27) and applied

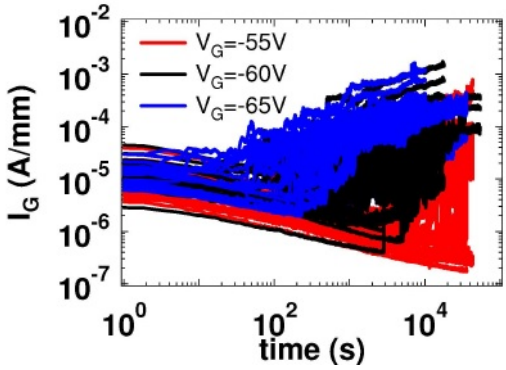

Figure 1.27: *Gate current monitored on 48 devices subjected to TDB experiments [79].*

time-dependent dielectric breakdown (TDDB) methodology to asses the GaN-based technologies under an OFF-state condition. By means of a statistical study, the time-to-failure can be fitted with a Weibull distribution (Figure 1.28), showing a low $\beta \sim 0.55$ at 273K and 473K. Furthermore, a power-law model was used to extrapolate the lifetime, as shown in Figure 1.29.

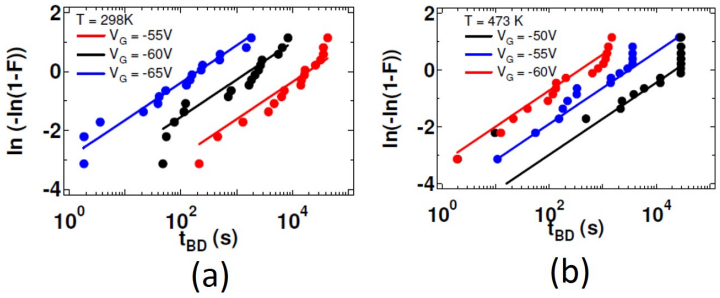

Figure 1.28: *Weibull plot of the time-to-breakdown (t_{BD}) distributions for the 3 TDB gate voltage conditions at different temperatures [79].*

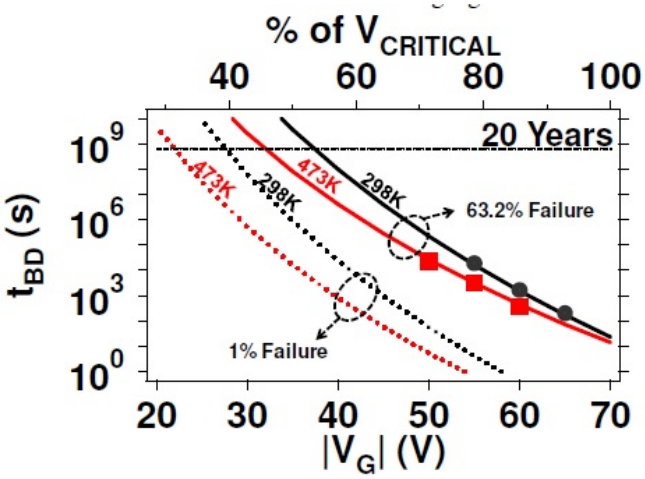

Figure 1.29: *Extrapolation of the t_{BD} towards low bias conditions at 298K (black) and 437K (red), with an example of lifetime extrapolation towards low percentage failures [79].*

1.4.3 SEMI-ON state related reliability issues

As shown in Figure 1.20, during the OFF-state to ON-state transition, especially hard switching, the transistor could operate at the critical current-voltage conditions where very high voltage and relatively high current level happen at the same time. This may lead to the generation of highly energetic electrons (hot electrons) which can cause not only long-term reliability issues [71] [83] but also enhance charge-trapping effects, leading to an instantaneous drop in dynamic performance [84].

In addition to the R_{ON} increase caused by high drain voltage in the OFF-state, Figure 1.30 shows a further worsening in the R_{ON} in the SEMI-ON-state when $V_{G,Q}$>V_{TH} (I_{DS}>10mA/mm). As shown in Figure 1.30(b), the R_{ON} increases as the drain current (I_{DS}) increases when the V_G is large than $\sim$ -4V (since the V_{TH} of this sample is $\sim$ -4V, the drain current (I_{DS}) starts conducting once the V_G is large than $\sim$ -4V). Therefore, the high correlation of the R_{ON} and the drain current density suggests that a further worsening in the R_{ON} is most probably due to a combination of high drain voltage and high source-to-drain current. In addition to the R_{ON} increase, this paper has also observed around 400mV V_{TH} shift.

Braga *et al*. showed that an appreciable density of electrons (conventionally referred to as hot electrons) can gain enough energy to overcome the 2DEG confinement even with

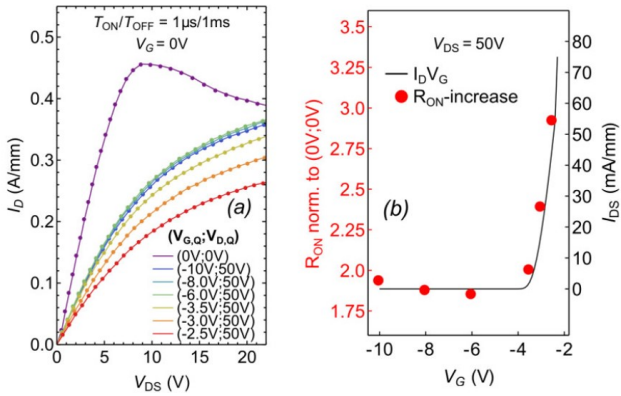

Figure 1.30: *Pulsed I_D–V_D characteristics acquired with constant quiescent $V_{D,Q}$, and multiple quiescent $V_{G,Q}$. Dynamic R_{ON} increase worsens as V_G>V_{TH} (a). Good correlation between I_{DS} and dynamic R_{ON} increase suggests the influence of hot-electron-related trapping mechanism (b) [85].*

moderated drain voltages. They are consequently deflected into the epitaxial structure, where they are trapped at crystallographic defect-states [86].

In sum, during SEMI-ON condition, the electrons accelerated by the electric field get trapped not only in the gate–to-drain access region but also underneath the gate region (Figure 1.31).

1.4.4 ON-state related reliability issues

In the past 20 years, a lot of literature has reported on the ON-state related reliability issues in Si CMOS and other advanced technologies, such as III-V, SiGe, etc. From these experiences, there are two main issues under the ON-state condition: 1) Forward gate bias time-dependent dielectric breakdown (TDDB) and 2) V_{TH} hysteresis after a positive forward-reverse gate sweep. However, these issues are less systematic being studied in GaN-based transistors, as shown in Figure 1.32. In order to develop long-term stability of E-mode GaN power devices, ON-state stability ought to be taken into account. Therefore, this thesis will focus on exploring the instabilities under ON-state conditions, and will further propose the physical mechanisms for understanding such instabilities.

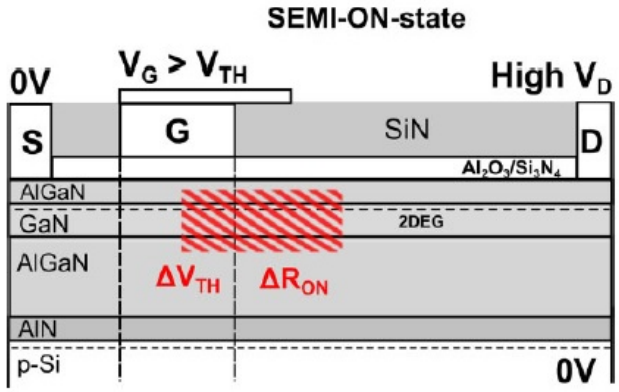

Figure 1.31: *During SEMI-ON-state, hot-electrons can overcome the 2DEG confinement due to a combination of high drain voltage and high drain current being further injected and trapped into epitaxial defect-states [85].*

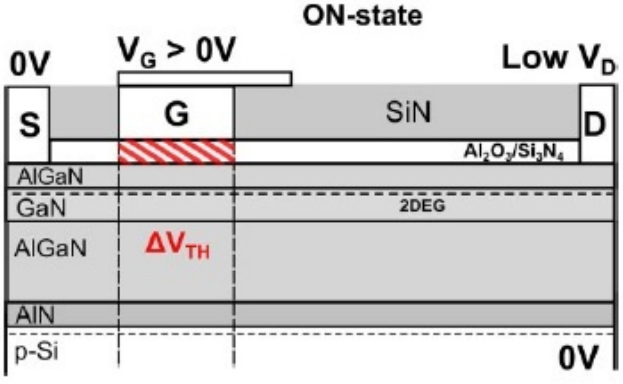

Figure 1.32: *During ON-state condition, electrons get trapped by interface states, border traps, or defects inside the gate dielectric, leading to V_{TH} instabilities [85].*

1.4.5 Conclusion

The reliability issues in GaN power devices have been reviewed. These issues have been divided into three parts: 1) OFF-state reliability, 2) SEMI-ON state reliability, and 3) ON-state reliability.

Regarding the OFF-state reliability, the OFF-state bias condition leads to the following issues: 1) current collapse and 2) OFF-state time-dependent gate edge degradation

With regard to the SEMI-ON state reliability, dynamic R_{ON} and V_{TH} shift could be observed at the same time.

As to the ON-state reliability, the relevant literature is rather limited and a systematic exploration is thus necessary, especially for the E-mode GaN-based devices. Therefore, this thesis will focus on the ON-state reliability in E-mode GaN-based devices.

1.5 Thesis content overview

1.5.1 Thesis objective

An overview of GaN-based material properties, device architectures, and reliability issues, has been discussed. It is commonly accepted that GaN-based devices show promising characteristics for power switching applications. However, the stability of GaN-based devices remains the main obstacle towards advancing to the level of mass production. Therefore, this thesis focuses on an exploration of the instability issues as well as understanding the degradation mechanisms, especially the issues related to the gate regions in recessed gate MIS-HEMTs/MIS-FETs and p-GaN AlGaN/GaN HEMTs.

1.5.2 Thesis outline

This thesis is arranged into the following chapters:

Chapter 2: Methodologies for exploring the reliability issues under the gate

This chapter provides an overview of the methodologies used in this thesis to explore the issues under the gate. First of all, in order to understand the strength of the gate dielectrics, time-dependent dielectric breakdown (TDDB) measurements are used. Detailed procedures and methodologies that include the statistic tools, such as Weibull distributions and lifetime calculations, are discussed. Secondly, in order to understand the mechanisms of V_{TH} hysteresis, interface characterization is needed. A frequency-

dependent conductance method is used to evaluate the conductance dispersion, further calculating the D_{it} with respect to the different trap levels. Thirdly, an advanced PBTI (positive bias temperature instability) technique, i.e. eMSM (extended-Measure-Stress-Measure), is used to study the stress-recovery phenomenon. By using this technique, V_{TH} hysteresis (with respect to different stress time and relaxation time) can be collected.

Chapter 3: Stability of D-mode AlGaN/GaN MIS-HEMTs on a 150mm Si substrate

D-mode AlGaN/GaN MIS-HEMTs with a bi-layer gate dielectric (*in-situ* SiN/Al_2O_3) have been successfully developed at imec for power switching applications. However, the ON-state reliability remains uncertain, including the time dependent dielectric breakdown and the forward gate bias stress, which are the main focus of evaluation in this chapter.

Chapter 4: Stability of E-mode recessed gate GaN MIS-FETs on a 200mm Si substrate

In order to develop E-mode GaN-based devices, recessed gates are used. However, recessing into the AlGaN barrier or GaN channel and non-native gate dielectric deposition might raise instability issues. Therefore, this chapter focuses on an exploration of the instability issues in D-mode recessed gate MIS-HEMTs and E-mode recessed gate MIS-FETs. Different reliability issues, including time dependent dielectric breakdown, V_{TH} hysteresis, and positive bias temperature instability (PBTI), are evaluated. The degradation mechanisms to explain these instabilities are proposed .

Chapter 5: Stability of E-mode p-GaN AlGaN/GaN HEMTs on a 200mm Si substrate

The other important architecture for developing an E-mode characteristic is the p-GaN gate on top of the AlGaN barrier. However, the p-GaN AlGaN/GaN HEMT is a relatively new concept, such that the reliability issues in this structure need to be explored. Therefore, this chapter focuses on the following: 1) the forward gate bias breakdown mechanisms and 2) the preliminary high forward gate bias stress.

Chapter 6: Conclusion and outlook

The final chapter summarizes the main results and contributions of this thesis. Furthermore, the suggestions for future research are briefly discussed.

Chapter 2

Methodologies for exploring reliability issues under the gate

2.1 Introduction

This chapter reviews the methodologies used in this thesis to explore the issues under the gate. First of all, an overview of time-dependent dielectric breakdown (TDDB) methodologies, including the t_{BD} extraction, percolation model, Weibull distribution, and lifetime calculation, are present. Secondly, a frequency-dependent conductance method is reviewed. This method is used to evaluate the conductance dispersion, further calculating the D_{it} with respect to the different trap levels. Thirdly, an advanced technique, i.e. eMSM (extended-Measure-Stress-Measure), is reviewed to study the PBTI with respect to different stress time and relaxation time.

2.2 Time-dependent dielectric breakdown (TDDB) experiment

2.2.1 Time-to-breakdown

Time-dependent dielectric breakdown has been extensively studied over the past decades in different technologies, e.g. Si-based, III-V, SiGe, etc., with different gate dielectrics, i.e. SiO_2, HfO_2, etc. [87] [88]. It has become one of the necessary reliability evaluations for studying the transistor's stability. Time-dependent dielectric breakdown (TDDB) experiments typically perform a CVS (Constant Voltage Stress) or CCS (Constant Current Stress) on a certain number of transistors or capacitors while monitoring current (voltage) variations with respect to time. In the case of CVS, the monitored current could suddenly increase after a period of stress time, as shown in Figure 2.1. This indicates that the gate dielectric loses its insulating properties and the time for this sudden increase is conventionally indicated as time-to-breakdown

(t_{BD}). When biasing at a high gate voltage, the high electric field induces a gradual degradation of the oxide, resulting in a sudden increase in its leakage current after a certain period of time (Figure 2.1). In the case of thick oxides (> 5nm; Figure 2.1 (a)), this phenomenon is followed immediately by the destruction of the dielectric layer (hard breakdown) due to thermal damage. On the other hand, for thin oxides (< 5nm; Figure 2.1 (b)), increases in the leakage current and its noise level, which indicate a "soft breakdown", can be observed before the dielectric destruction [87].

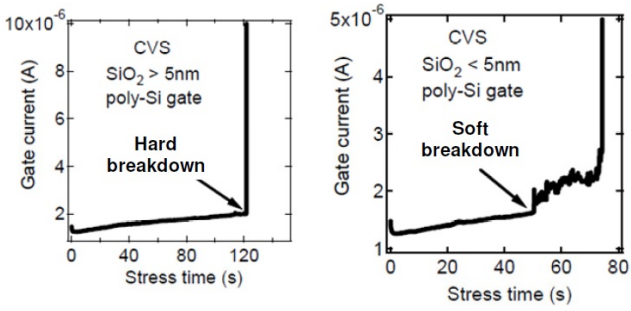

Figure 2.1: *Current through an oxide during constant voltage stress (CVS) in the case of thick (a) and thin (b) oxide thickness [88]. In the case of thin oxide (b), soft breakdown, which shows the gate leakage current increases and becomes noisy, occurs before the final destructive breakdown. In the case of thick oxide (a), only the final destructive breakdown (hard breakdown) is observed.*

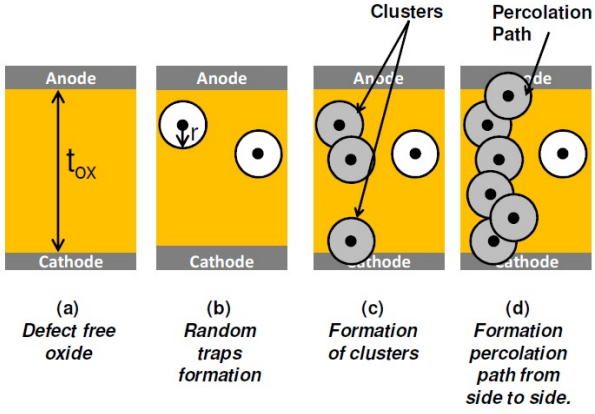

Figure 2.2: *Schematic of the formation of percolation during a CVS [26].*

Time-dependent dielectric breakdown has been well explained by the percolation model [87], as shown in Figure 2.2. Initially, there are no defects inside the oxide (Figure 2.2 (a)). The leakage conduction mechanism in SiO_2 dielectric is mainly due to Fowler–Nordheim tunneling or direct tunneling. During a stress, a random creation of traps occurs; each trap can be modeled with a sphere of radius r (Figure 2.2 (b)). A sphere of two traps could form a conduction path when the two traps overlap (Figure 2.2 (c)). After a certain period of stress time, more and more random traps are generated (Figure 2.2 (d)), and a percolation path is formed between the anode and cathode. Under this situation, electrons can flow via this conduction path, leading to a sudden increase in the current, further resulting in oxide breakdown.

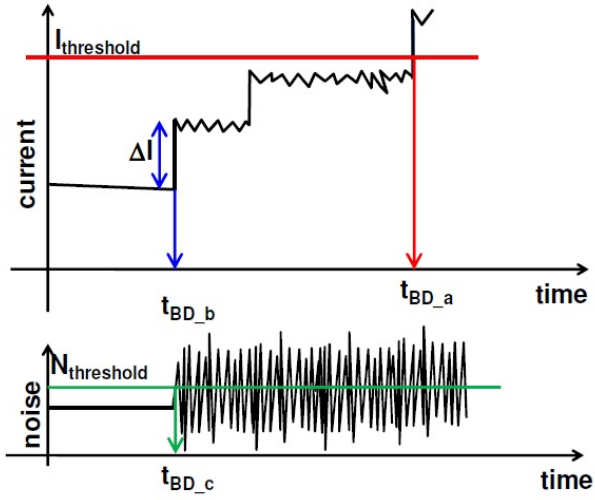

Figure 2.3: *Schematic of the current-time traces and its noise during a CVS. Time-to-breakdown (t_{BD}) can be extracted based on different t_{BD} definitions: 1) t_{BD_a} is extracted when the current increases beyond a threshold ($I_{threshold}$); 2) t_{BD_b} is extracted when a current step is larger than a defined value (ΔI); and 3) t_{BD_c} is extracted when the noise of the current goes beyond a threshold ($N_{threshold}$) [26].*

The t_{BD} values are extracted from the recorded current-time (I-t) trace during a stress. This can be performed by means of a manual extraction or using special software. At imec, automatic TDDB data analysis "TeDDy Bear" has been developed to address this issue. There are different ways to extract the t_{BD}-values [88], which is mainly due to the different definitions of t_{BD}. As schematically shown in Figure 2.3, t_{BD} can be defined:

a) when the monitored current increases beyond a defined current threshold ($I_{threshold}$);

b) when the monitored current presents a step (ΔI) higher than a defined value;

c) when the noise level of the monitored current increases beyond ($N_{threshold}$) a certain value.

The easiest method is the first detection (a), which is used to detect the hard breakdown phenomenon rather than the soft breakdown phenomenon. However, the formation of single or multiple breakdown paths is not clear in the first detection method. Therefore, this extraction method (t_{BD_a}) in Figure 2.3 cannot indicate precisely the formation of the first percolation path. The second detection method (b) is used to detect the first current step beyond a defined criterion. This method could identify the time for forming the first percolation path (t_{BD_b}) in Figure 2.3 if and only if a proper criterion (step-height) for detection is defined. Please note that this defined criterion is empirical for each experiment, which needs to be carefully selected. The third detection method (c), the most complicated one, is used to detect the noise of the I-t since the first percolation leads to an increase in the noise (Figure 2.3). The t_{BD} is extracted when the noise amplitude is higher than a defined threshold value. Normally, the t_{BD} extraction, based on the current step analysis (b), has been widely used. A specific software ("TeDDy Bear") has been created and optimized to implement this method [89].

2.2.2 Statistical properties and data analysis

In the previous section, the phenomenon and physical mechanism of TDDB as well as the extraction of t_{BD}-values from experimental I-t traces have been discussed. Under the applied stress condition, these t_{BD} data from the extraction represent the time necessary to form the first percolation path on each measured sample. In a realistic case, the percolation path is not formed at the same time (identical t_{BD}) in each device, as in the case of the identical light bulbs which would not fail at the same time. Actually, the t_{BD} is a statistically distributed parameter, which can be plotted in a histogram plot. However, the cumulative failure distribution function F(t) is more useful for providing a further in-depth analysis, which can be calculated from an appropriate fitting of the cumulative distribution of the t_{BD} values. Generally, the cumulative failure distribution function F(t) describes the probability that a device fails at or before a certain generic time t; F(t) can assume values between 0 and 1. Since everything will fail in the end, F(t) tends towards 1 while t approaches infinite. In the specific case of gate dielectric degradation, F(t) indicates the probability for the formation of a percolation path before or at the time t under a given stress condition. The t_{BD}-data of SiO_2 dielectric have been shown to be distributed according to the Weibull statistic [87–89]. The cumulative Weibull distribution function F(t) is defined as follows:

$$F(t) = 1 - exp[-(\frac{t-\gamma}{\eta})^{\beta}] \tag{2.1}$$

where β is the shape parameter, η is the scale factor or 63.2% value, and γ is the time delay or burn-in time (in most of the experiments $\gamma = 0$). Assuming $\gamma = 0$, the Weibull failure distribution can easily be rewritten as:

$$ln[-ln(1 - F(t))] = \beta ln(t) - \beta ln(\eta) \tag{2.2}$$

A plot of *ln(-ln(1-F(t)) vs. ln(t)* yields a straight line with a slope β and intercept *ln(η)*, which can be calculated from a suitable fitting. A semilog plot of *ln(-ln(1-F(t))* vs *ln(t)* is commonly called Weibull plot. In order to estimate the function F(t), it is necessary first to calculate the cumulative failure distribution of the t_{BD} data $F(t_{BD\_i})$. This starts with ordering the t_{BD} from the smallest to the largest value, followed by applying an appropriate ranking algorithm. The most appropriate ranking algorithm is the median ranking [88] [89], which is used to obtain an estimated value of the $F(t_{BD\_i})$ with each failure time t_{BD_i}. These values are subsequently fitted to obtain F(t). The Benard approximation is typically used to simplify the calculation of median ranking, as shown in the following:

$$F(t_{\mathrm{BD\_i}}) = \frac{i - 0.3}{n + 0.4} \tag{2.3}$$

where *i* is the number of failed devices, and *n* is the total number of tested devices.

Furthermore, by plotting the $(t_{BD\_i}, F(t_{BD\_i}))$ in a Weibull plot, it is possible to evaluate whether the data follow the Weibull distribution or not. The data which follow Weibull distribution approximately fit to a straight line, as indicated in equation 2.2. The data analysis procedure for the TDDB experiments can be summarized in the following steps:

a) Extraction of the t_{BD} data from each recorded I-t trace during a CVS test (Figure 2.4 (a)). The t_{BD} can be defined when the current exhibits a step larger than a defined value.

b) Ordering of the t_{BD}-values from the smallest to the largest, and extraction of the $F(t_{BD\_i})$ by means of the Benard approximation for median ranking (Figure 2.4 (b)).

c) Plot the $F(t_{BD\_i})$ data in a Weibull plot (Figure 2.4 (c)) and apply a suitable fitting procedure. This procedure extracts the two parameters β and η from the associated Weibull F(t) function.

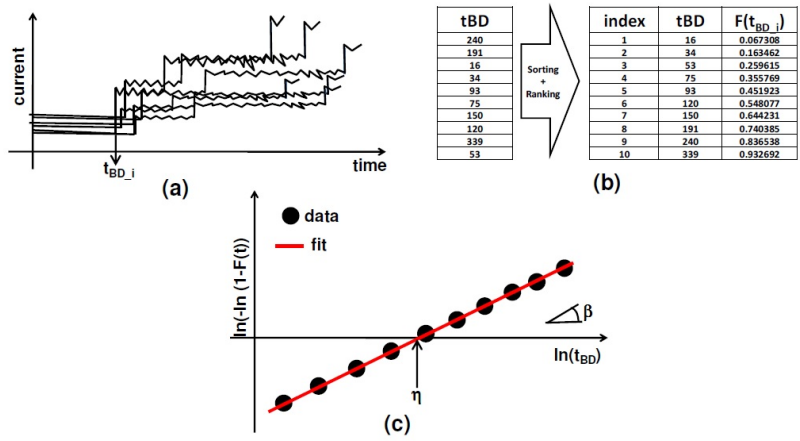

Figure 2.4: *An example of analysis in a TDDB experiment: (a) t_{BD}-values are extracted from the recorded I-t traces during a CVS; (b) first, the obtained t_{BD}-values are ordered from the smallest to the highest, second, the cumulative failure distribution $F(t_{BD\_i})$ is calculated using a median ranking algorithm approximated with a Benard formula; (c) $F(t_{BD\_i})$ is shown in a Weibull plot; a suitable fitting algorithm can extract the associated Weibull distribution best describing the data if the data follow the Weibull distribution. The two parameters of the Weibull distribution, β and η, are shown in (c) [26].*

R. Degraeve and T. Kauerauf [88] [89] have shown that the maximum likelihood (ML) method is the most suitable procedure for fitting statistical reliability distributions. By inputting the empirical data, this method can extract the distribution parameters that most likely represent the data given as input. In the specific case of the TDDB experiment, the ML algorithm has been used to extract the Weibull parameters β and η that most likely represent the distribution of the measured t_{BD}-data. Moreover, the censured data, time-outs, and earlier failures, which imply valuable information in the reliability analysis, are also taken into account in this method. The ML algorithm has been implemented and optimized in the software ("TeDDy Bear") and more information about the ML method can be found elsewhere [88] [89].

Based on the theory of time-dependent breakdown, the breakdown path should be formed randomly in the device area. This indicates that large area devices would be prone to statistically fail earlier than small area devices with identical gate dielectric thickness. Therefore, the F(t) of different device areas with the same gate dielectric thickness follows the area scaling law. In terms of a large area capacitor A_1, this can be considered to have been formed by n small area A_2 capacitors. By using the property

of series reliability systems (i.e. a system fails if any of its component fails), it can be shown [89] that the Weibull function F(t) of capacitors with area A_1 ($F_{A1(t)}$) can be expressed as a function of the F(t) of capacitors with area A_2 ($F_{A2(t)}$) as follows:

$$ln[-ln(1-F_{A_1}(t))] = ln(\frac{A_2}{A_1}) + ln[-ln(1-F_{A_2}(t))] \tag{2.4}$$

Consequently, it is easy to extract by means of the following:

$$ln[-ln(1-F_{A_1}(t))] = ln(\frac{A_2}{A_1}) + \beta\ ln(t) - \beta\ ln(\eta_2) = \beta ln(t) - \beta ln(\eta_1) \tag{2.5}$$

where

$$\eta_1 = \eta_2(\frac{A_2}{A_1})^{1/\beta} \tag{2.6}$$

Therefore, the Weibull plot of the F(t) of two sets of capacitors with a different area A_1 and A_2 and with identical gate dielectric thickness renders them parallel to each other (i.e. the same β) and only vertically shifted by $(A_2/A_1)^{1/\beta}$, as defined in equation 2.6.

By performing TDDB experiments with a different device area A_i, it is possible to examine whether extrinsic or intrinsic reliability issues lead to the time dependent dielectric breakdown.

By using equation 2.4, it is possible to refer each A_i area device to a common reference area A_1. In case of homogenous stress and degradation, the distributions scale vertically and are nicely lined up, as experimentally shown in Figure 2.5 [88].

On the other hand, the leakage path could easily be formed in a specific spot due to a process-induced defect or weakness of the dielectric in a specific location, such that there is no difference between small and large area devices. In this case, the area scaling could not be applied and the distribution will not vertically align.

As mentioned above, the shape parameter β of the Weibull distribution represents the slope of the F(t) function, as shown in a Weibull plot. Therefore, β can directly give an indication on the spread of the measured data: a large β value indicates a smaller spread of the data and vice versa.

It has also been shown that the parameter β is strongly related to the number of defects forming the percolation path [88].

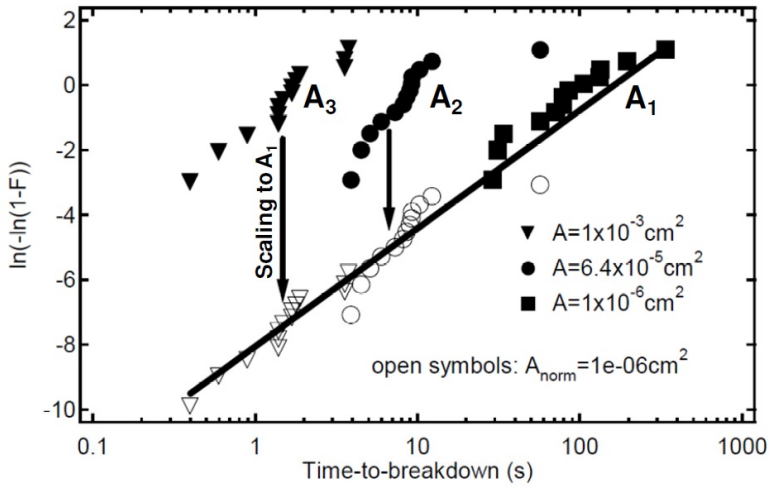

Figure 2.5: *In the case of uniform degradation, the distribution of t_{BD}-values measured on devices with three different areas (A_1, A_2 and A_3) nicely lines up to one distribution once they are scaled to a single reference area (A_1 in this case) [88].*

$$\beta = m \times N \tag{2.7}$$

where *m* is the trap generation rate and *N* is the number of defects needed to form the percolation path. *m* is defined at any time the oxide defect (D_{ot}) density (in the ideal case of zero initial defects), as shown in the following:

$$D_{\text{ot}} = c \times t_{stress}^{m} \tag{2.8}$$

where c is a parameter function of the stress condition and t_{stress} is the stress time.

Note that it has been experimentally observed that *m* is independent of the dielectrics (SiO_2, SiON, HfSiON and HfO_2), and that *m* is in the range from 0.35 and 0.4 [89]. Furthermore, by using equation 2.7 and *m*= 0.35 - 0.4, it is possible to plot the expected (intrinsic) β_{tBD} as a function of the number of traps in forming the percolation path (Figure 2.6).

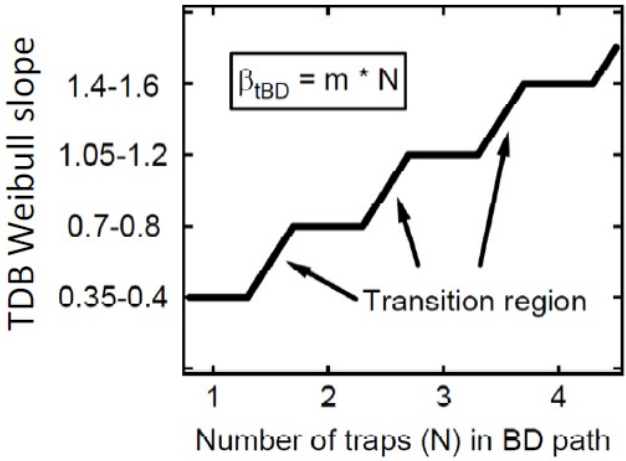

Figure 2.6: *The t_{BD}-Weibull slope (β_{tBD}) versus the number of traps N in forming the percolation path. Note that certain event to form the the percolation path could be caused by either N or N+1 traps, showing a transition region between the different levels [88].*

2.2.3 Lifetime extrapolation

By performing TDDB experiments under different stress conditions, the Weibull failure distribution and its associated β and η can be extracted from each experiment.

Note that β is intrinsically related to the gate dielectric thickness, and that the failure distributions F(t) with respect to each stress condition are parallel to each other and only shifted by the η factor, which is a function of the applied condition, as shown in Figure 2.7.

Therefore, the Weibull parameter η (i.e. the time at which 63.2% of the gate dielectric devices fail) is closely linked to the applied stress condition. By performing TDDB experiments under different stress conditions, the plot η versus the applied conditions can be built (e.g. voltage used during CVS), as shown in Figure 2.7 (b). By fitting this relation with a model, it is possible to predict when 63.2% of the gate dielectric devices fail under actual operating conditions. Note that in order to observe the failures within a reasonable experimental time, the stress conditions during TDDB experiments are always larger than the actual operating conditions so as to accelerate the degradation. Furthermore, by applying the area scaling law (Equation 2.6), the lifetime of any arbitrary area device can be predicted.

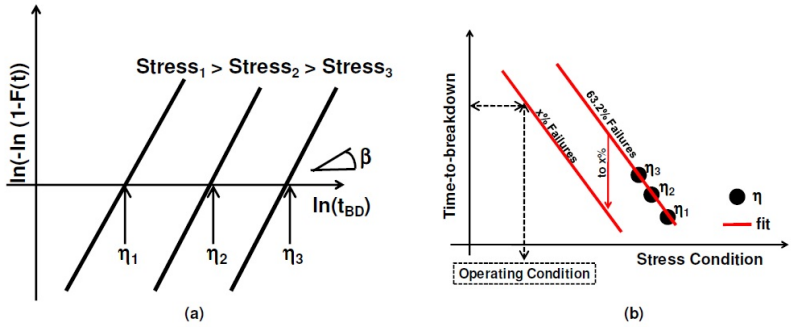

Figure 2.7: *(a) Schematic of a Weibull plot associated with TDDB experiments under 3 different stress conditions, resulting in η_1, η_2, and η_3. (b) Illustration of the time-to-breakdown long-term extrapolation. First of all, based on η values (63.2% failure), a suitable fit function can predict the time-to-breakdown under specific conditions. Of those 63.2% of failures, it is easier to scale them to an x% failure level, and consequently to determine the probability that x% of the population fail under certain operating condition and vice-versa [88].*

Additionally, based on the time when 63.2% of the population fail, it is easy to extract the time corresponding to the failure of an arbitrary percentage x% of the population (e.g. $t_{1\%}$ or $t_{10\%}$) for a given operating condition (Figure 2.7 (b)). Conversely, given the expected lifetime for x% of the population, it is also possible to determine the operating conditions that would guarantee it (Figure 2.7 (b)).

The key in the lifetime extrapolation procedure is the fitting model. The fitting model allows for the prediction of lifetime based on an accelerated stress condition. The so-called "1/E-model" or "E-model" is normally adopted with $t_{ox} > 5$ nm [87]. Both models link the time-to-breakdown with the oxide field (E_{ox}). Indeed, for $t_{ox} > 5$ nm, the electrons are injected by FN-tunnelling into the conduction band of the oxide. In this case, E_{ox} uniquely determines the electron energy at the anode (Figure 2.8 (a)) which triggers the oxide's degradation.

The extrapolation law of the 1/E-model is shown in the following:

$$t_{BD} = \tau_0 \, exp(\frac{G}{E_{ox}}) \tag{2.9}$$

where τ_0 and G are constants. Instead, in the case of the E-model, the extrapolation law is formulated as follows:

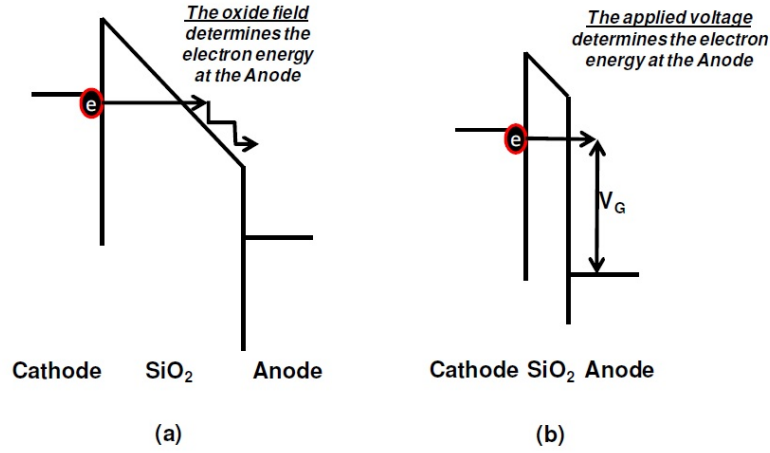

Figure 2.8: *Schematic band diagram in case of (a) thick oxide (t_{ox} > 5 nm) and (b) thin oxide (t_{ox} < 5 nm). In the first case, the electron energy at the anode is determined by the oxide field, whereas in the second case it is determined by the applied bias conditions [26].*

$$t_{BD} = t_0 \, exp(-\gamma \times E_{ox}) \tag{2.10}$$

where t_0 and γ are constants.

Although both models can fit the experimental data very well, the long-term extractions are diverse, which cannot be measured in reality (e.g. 20 years). However, there is no consensus about which model is best so far and the debate is still on-going. In the case of t_{ox} < 5 nm, the electrons can be tunneled directly through the oxide to the conduction band of the semiconductor. In this case, the electron energy released at the anode is determined by the voltage difference between anode and cathode, which is the applied voltage condition V_G (Figure 2.8 (b)). So, the electric field-based models have to be replaced by voltage-based models [87] [89]. The most used voltage-based models are the "exponential V_G model" and "V_G power law model". The exponential V_G model is defined as:

$$t_{BD} = t_0 exp(-\gamma \times V_G) \tag{2.11}$$

where t_0 and γ are constants.

The exponential V_G model has been initially used to predict the lifetime in devices with very thin oxides. Although it fits the experimental data well, the correctness of the predicted lifetime was debated [88] since this model predicts a finite lifetime at V_G = 0 V. However, regarding typical Si CMOS technologies, the failure time should be infinite when the device is biased at V_G = 0 V.

On the other hand, the V_G power law model can both fit the experimental data well and is able to avoid inconsistencies as mentioned above [88]. The extrapolation law based on this model is defined as:

$$t_{BD} = k_0 \times V_G^{-n} \tag{2.12}$$

where k_0 and n are constants.

From equation 2.12, this model correctly predicts an infinite lifetime at V_G = 0V. Furthermore, trap generation follows the same power law [88], supporting the power law model in lifetime calculation. Note that temperature, which can accelerate the degradation phenomenon, definitely plays an important role in the oxide degradation. Under the same stress conditions, η extracted at room temperature is larger than η extracted at high temperature [90]. Furthermore, the exponent of the power law model n (equation 2.12) for lifetime extrapolation can change at different temperatures [90]. The relation between t_{BD} and temperature is not obvious. But, TDDB experiments are often performed at the operating target temperature in order to guarantee the correct lifetime extrapolation, which can include the temperature effect on the t_{BD}-data.

2.3 Interface characterization methods

Capacitance- and conductance-based techniques have been extensively used in Si CMOS technology to characterize the parameters of Si MOSFETs and MOS capacitors, such as the flat-band voltage, effective oxide thickness, work function, fixed charge, doping level, density of interface traps, etc. Among those, the interface state density (D_{it}) is most critical to quantify the electrical quality of the interface between a semiconductor and the gate dielectric (channel/gate dielectric) interface. As mentioned in chapter 1, when considering a MIS-HEMT or fully recessed gate MIS-FET, a non-native gate dielectric on top of an AlGaN barrier or GaN channel as well as the recessed damages could lead to instability of the transistors. Therefore, it is crucial to characterize the interface below the gate dielectric to compare it with the different processes. Various interface characterization methods have been developed for a

while now, including low frequency (quasi-static) methods, Terman method, combined high-low frequency method, charge pumping, deep level transient spectroscopy, and frequency-dependent conductance method [91].

Among these methods, the frequency-conductance method is one of the most sensitive methods for determining D_{it} [92]. The conductance method was proposed by Nicollian and Goetzberger in 1967. Interface trap densities of $10^9\ cm^{-2}eV^{-1}$ and lower can be measured. It is also one of the most-developed methods because it can determine D_{it} in the depletion and weak inversion part of the bandgap, capture cross sections of majority carriers, interface trap time constants, and surface potential fluctuations. The method is based on measuring the equivalent parallel conductance (G_p) of a MOS capacitor as a function of gate bias and frequency. The parallel conductance (G_p) is measured as a result of the loss due to interface trap capture and emission of carriers. The magnitude of the conductance peaks relates to the interface trap density.

A simplified equivalent circuit of an MOS-C for the conductance method is shown in Figure 2.9 (a). It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_s, and the interface trap capacitance C_{it}. The capture-emission of carriers by D_{it} is a lossy process, represented by the resistance R_{it}. It is convenient to replace the circuit in Figure 2.9 (a) by that in Fig. 2.9(b), where C_p and G_p are given by:

$$C_p = C_s + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \tag{2.13}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{(1 + (\omega\tau_{it})^2)} \tag{2.14}$$

where $C_{it} = q^2 D_{\mathrm{it}}$, $\omega = 2\pi f$ (f = measurement frequency) and $\tau_{\mathrm{it}} = R_{\mathrm{it}}C_{\mathrm{it}}$, the interface trap time constant, given by $\tau_{\mathrm{it,electron}} = [v_{\mathrm{th}}\sigma_{\mathrm{e}}N_{\mathrm{C}}exp(-q(E_C - E_t)/kT)]^{-1}$ or $\tau_{\mathrm{it,hole}} = [v_{\mathrm{th}}\sigma_{\mathrm{h}}N_{\mathrm{A}}exp(-q(E_t - E_V)/kT)]^{-1}$, where σ_{e} and σ_{h} are the capture cross section for electrons and holes, respectively, and $E_{\mathrm{C}} - E_{\mathrm{t}}$ and $E_{\mathrm{t}} - E_{\mathrm{V}}$ indicate the trap energy below the conduction band and the trap energy above the valence band, respectively. Dividing G_p by ω makes Eq. 2.14 symmetrical in $\omega\tau_{it}$. Equations 2.13 and 2.14 are for interface traps with a single energy level in the band gap. Interface traps at the SiO_2-Si interface are, however, continuously distributed in energy throughout the Si band gap. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and the normalized conductance, as shown in Equation 2.15 [92].

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2(\omega\tau_{it})} ln[1 + (\omega\tau_{it})^2] \tag{2.15}$$

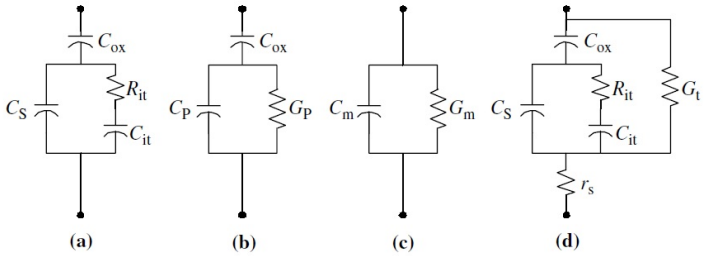

Figure 2.9: *Equivalent circuits for conductance measurements: (a) MOS-C with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), (c) measured circuit, (d) including series r_s resistance and tunnel conductance G_t [91].*

Equations 2.14 and 2.15 show that the conductance is easier to interpret than the capacitance because Eq. 2.14 does not require C_S. The conductance is measured as a function of frequency and plotted as G_P/ω versus ω. G_P/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2G_P/q\omega$. For Equation 2.15 we find $\omega \approx 2/\tau_{it}$ and D_{it}=2.5$\times G_P/q\omega$ at the maximum. Hence, we determine D_{it} from the maximum G_P/ω and determine τ_{it} from ω at the peak conductance location on the ω-axis. G_P/ω versus f plot is calculated according to Eqs. 2.13 and 2.14. The experimental G_P/ω versus ω curve is generally broader than predicted by Eq. 2.15, as shown in Figure 2.10. This is due to the fact that interface trap time constant dispersion caused surface potential fluctuations as a result of non-uniformities in oxide charge and interface traps as well as doping density. Therefore, such broader curve, which is typically measured as standard deviation σ_s, needs to be taken into account. The standard deviation σ_s is a measure of the width of curve in Figure 2.11. The width of the G_P/ω versus log frequency curve along the frequency axis is dependent only on σ_S. However, the G_P/ω versus gate bias curve will be spread over a bias range determined by σ_S and D_{it}. The interface trap contribution to the width is caused by the change in occupancy with the gate bias.

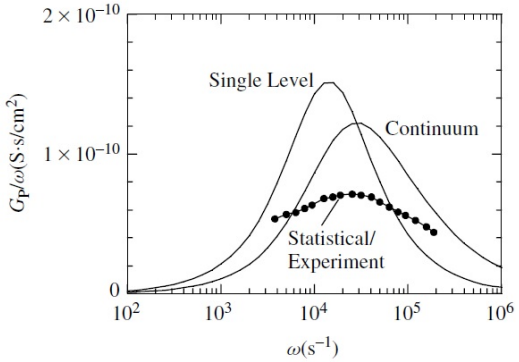

Figure 2.10: *G_P/ω versus ω for a single level [Eq. 2.14], a continuum [Eq. 2.15], and experimental data [93].*

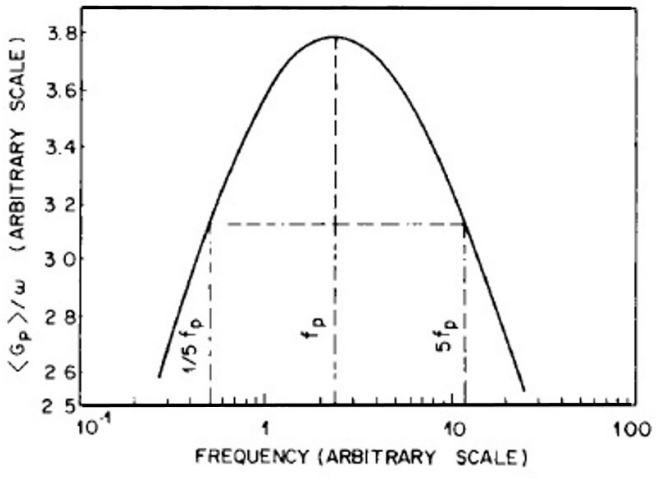

Figure 2.11: *A typical G_p/ω versus the frequency curve obtained from measurement, where f_p is the frequency corresponding to the peak value of G_p/ω. The points at $f_p/5$ and $5f_p$ define the width of the curve on the low and high frequency side of f_p, respectively [94].*

Figure 2.11 shows a typical G_p/ω versus log frequency curve from which σ_S is to be determined. The procedure is to measure the amplitude change of this curve either between the points f_p and f_p/n or between f_p and nf_p where f_p is the frequency corresponding to the peak value of G_p/ω. Figure 2.12 plots the ratio between $[G_p/\omega]_{f_p/n}$

and $[G_p/\omega]_{f_p}$ and the ration between $[G_p/\omega]_{nf_p}$ and $[G_p/\omega]_{f_p}$. Choosing n=5 is reasonable because generally the values of G_p/ω at these frequencies will not be too low, close to the peak values, so that accurate values of these ratios can be found. Using the experimental ratios, the corresponding σ_S is found from Figure 2.12.

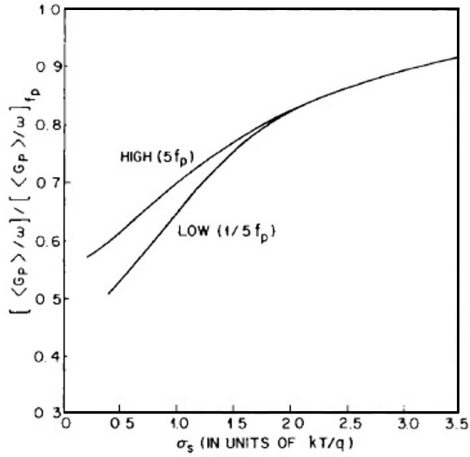

Figure 2.12: *Plot of $[G_p/\omega]/[G_p/\omega]f_p$ versus standard deviation of band bending [94].*

The asymmetry of the G_p/ω versus log frequency curves about f_p results in high and low frequency ratios that differ in values of σ_S (below 1.8), as shown in Figure 2.12. This asymmetry is due to the influence of the Fermi function weight factor on the loss. For values of σ_S greater than 1.8, the Gaussian weight factor dominates [94], making the G_p/ω versus log frequency curves symmetrical around f_p, indicated by the merging of the $f_p/5$ and $5f_p$ curves in Figure 2.12.

To calculate D_{it}, the peak value $[G_p/\omega]f_p$ at $\xi=\xi_p$ can expressed as follows [94]:

$$\left(\frac{< G_p >}{\omega}\right)_{f_p} = qD_{it}f_D(\sigma_s) \tag{2.16}$$

Solving 2.16 for D_{it}, we obtain

$$D_{it} = \left(\frac{< G_p >}{\omega}\right)[f_D(\sigma_S)q]^{-1} \tag{2.17}$$

where

$$f_D(\sigma_S) = \frac{(2\pi\sigma_S^2)^{-1/2}}{2\xi_P} \int_{\infty}^{\infty} exp\big(-\frac{\eta^2}{2\sigma_S^2}\big) exp(-\eta) ln(1+\xi_P^2 exp2\eta) d\eta \quad (2.18)$$

Equation 2.18 is plotted in Figure 2.13, which is used with Equation 2.17 to determine D_{it}, once σ_S is determined from Figure 2.12.

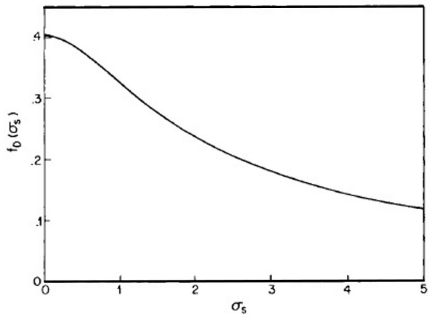

Figure 2.13: *Plot of the universal function $f_D(\sigma_S)$ defined in Equation 2.18 as a function of σ_S; f_D is used in Equation 2.17 to calculate the interface trap level density [94].*

2.4 V_{TH} shift and Positive Bias Temperature Instability (PBTI) characterization

2.4.1 V_{TH} shift characterization

Typical forward-reverse gate bias sweep

V_{TH} hysteresis is typically characterized by a forward-reverse gate voltage sweep, as shown in Figure 2.14. This method makes it possible to quickly evaluate the V_{TH} hysteresis from lot to lot.

V_{TH} shift during a positive gate bias stress

On top of the typical forward-reverse gate bias sweep, one may monitor the V_{TH} shift during a positive gate bias. This typical procedure includes a constant gate bias

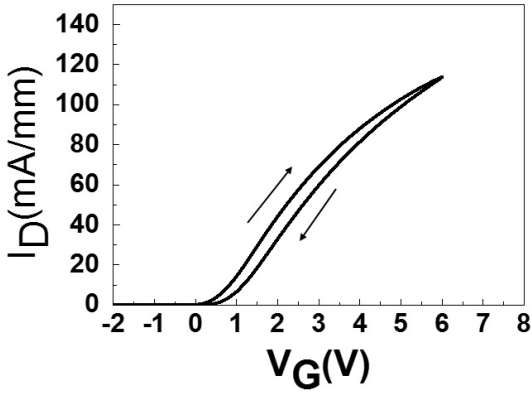

Figure 2.14: *An example of forward-reverse V_{TH} hysteresis characterization.*

stress for a certain period and several interrupted V_{TH} characterizations (typical I_D-V_G characterization) (Figure 2.15 and Figure 2.16). This methodology could provide the V_{TH} shift with respect to the stress time. However, relaxation could happen during each I_D-V_G characterization and the condition of I_D-V_G characterization (V_G and V_D) needs to be carefully selected in order to avoid any extra degradation.

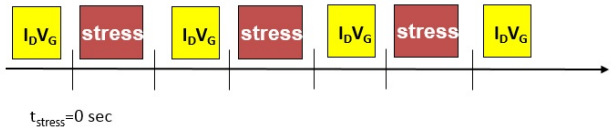

Figure 2.15: *V_{TH} shift during a positive gate bias stress with the interrupted V_{TH} characterization.*

2.4.2 Positive Bias Temperature Instability (PBTI) characterization

Note that the most important characteristics of BTI are time-dependent V_{TH} shift and recovery, which cannot be extracted from a simple forward-reverse gate voltage sweep or a positive gate bias stress with the interruption of V_{TH} characterization. An extended Measure-Stress-Measure is developed to characterize bias temperature instability (BTI),

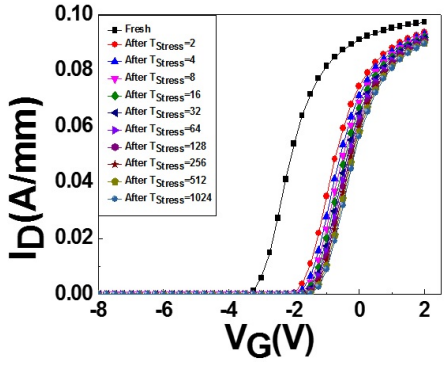

Figure 2.16: *An example of V_{TH} characterization during a positive gate bias stress.*

which can capture both the degradation and relaxation behavior. An overview of this technique is given in the following.

extended Measure-Stress-Measure (eMSM) technique

In order to further understand the BTI, a set of stress/recovery tests was proposed and performed by Kaczer *et al.* [95], which is called eMSM (extended Measure-Stress-Measure) technique, an evolution from Measure-Stress-Measure [96], as shown in Figure 2.17.

During each stress, the device is tested at two different periods, comprising of alternating stress phases at V_{stress} and measure (or "relaxation") phases at $V_{meas} \approx V_{TH0}$. A small V_D (e.g. 50mV) is always applied to allow for recording the transistor current during the entire experiment. Each measurement phase is designed to collect a maximum amount of BTI relaxation information in a time-efficient way. Typically, relaxation is recorded over 4 time-decades from 1ms to 10s.

First of all, a full I_D-V_G characterization was conducted in a fresh reference device to identify the reference threshold voltage (V_{TH0}). Secondly, in the test devices, in order to avoid pre-stressing the device during the initial I_D-V_G characterization sweep, the I_D-V_G was only measured up to the V_{TH0}. After each stress, a single I_D is measured while V_G is biased at V_{TH0}, allowing V_{TH} to be converted from the I_D decreases (Figure 2.18). Note that "r1", "r2", "r3", and "log" represent different logarithmic sampling times to efficiently cover the relaxation period.

Since only a single I_D needs to be obtained (instead of a range of I_D under different gate biases), this approach is faster than the I_D-V_G sweep, which can significantly limit

relaxation. However, this technique still has a measurement delay in the range of 1ms when implemented with standard off-the-shelf DC measurement instrument, and it does not account for the unknown fraction of recovery already in progress.

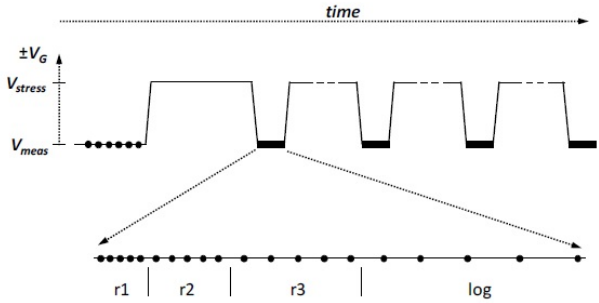

Figure 2.17: *Sketch of the working principle of the eMSM technique as introduced by Kaczer et al. [95]. Each 'measure' phase is designed to collect maximum information about relaxation. The segments of each relaxation phase, labeled as 'r1, r2, r3, log', represent different current measurement sampling rates that are used to efficiently cover the logarithmic time scales.*

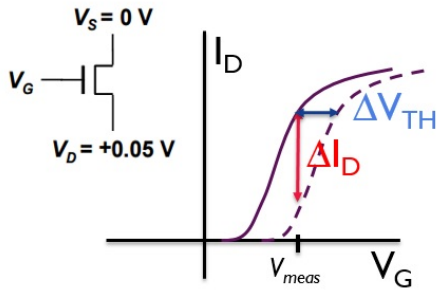

Figure 2.18: *Illustration of ΔI_D-ΔV_{TH} conversion based on the I_D-V_G characteristic of the fresh device.*

Figure 2.19 reports typical relaxation information obtained via the eMSM technique. A complete set of relaxation transients recorded after a corresponding set of stress phases with increasing duration is shown in Figure 2.20

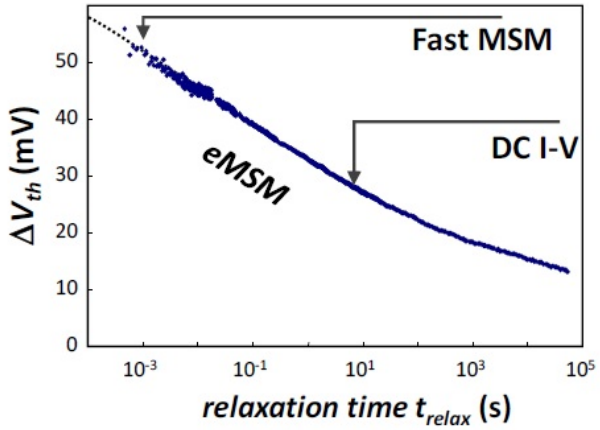

Figure 2.19: *A typical transient recorded using the eMSM technique, further providing information about NBTI relaxation over several time-decades. The delayed information regarding the fast MSM and typical I_D-V_G characteristic were shown in the graph for comparison [97].*

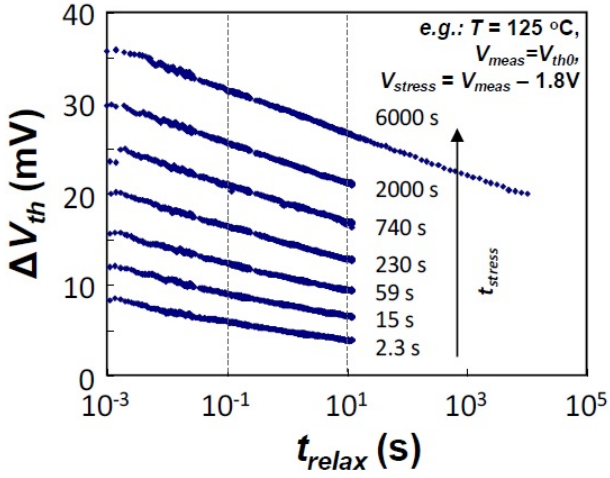

Figure 2.20: *A set of relaxation transients recorded after each stress phase with a different gate bias [97].*

Although eMSM is originally developed to study the NBTI, the technique has also been

applied to assess the positive temperature instability (PBTI) in III-V technologies [98]. The V_{TH} shift (Figure 2.21) during each PBTI stress can be collected as well as the relaxation information (Figure 2.22).

The ΔV_{TH} during the stress typically follows a power law [98–101], as shown in the Equation 2.19. The red dashed lines in Figure 2.21 also shows that the experimental data can be fitted with this power law well. Therefore, this power law can be used to extrapolate the lifetime when the ΔV_{TH} reaches a criteria.

$$\Delta V_{\mathrm{TH}} = A_0 (V_{\mathrm{G}} - V_{\mathrm{TH0}})^{\gamma} t_{stress}^{n} \tag{2.19}$$

where A_0 is the power-law prefactor, γ is the voltage exponent, and n is the time exponent.

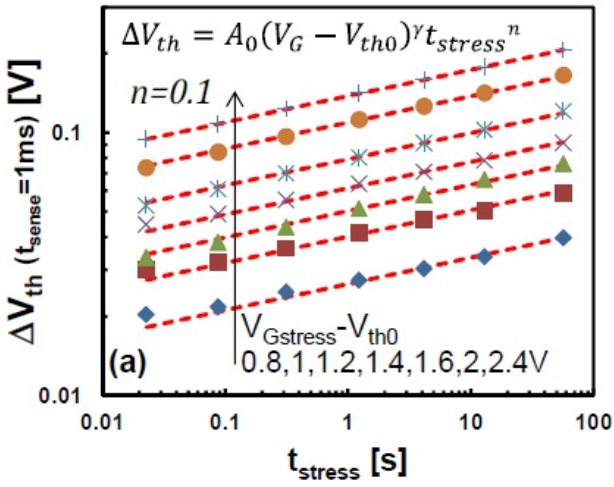

Figure 2.21: *ΔV_{TH} (t_{stress}) traces measured with the eMSM technique (t_{sense}=1ms) for varying overdrive stress voltages in InGaAs devices [98].*

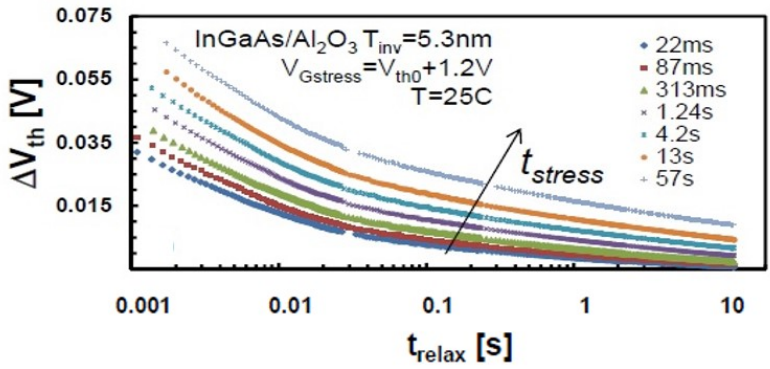

Figure 2.22: ΔV_{TH} *(typical set of PBTI relaxation traces measured on InGaAs/Al_2O_3 devices) [98].*

2.5 Summary of this chapter

In this chapter, the methodologies for exploring reliability issues under the gate have been reviewed. First of all, the details of the time-dependent dielectric breakdown (TDDB) experiments and their data analysis have been discussed. Several key points, including t_{BD} extraction, Weibull plot, the meaning of β and η, and the different lifetime models, have been pointed out. These analyses will be further applied to D-mode and E-mode GaN transistors, as shown in chapters 3 and 4.

Secondly, the interface state density (D_{it}) is one of the key features for evaluating the interface quality between a gate dielectric and a semiconductor. The most complete method for evaluating interface state density (D_{it}) is the frequency-dependent conductance method, which has been reviewed in this chapter. This method will be applied to the GaN-based transistor in chapter 4 to understand the impacts of different gate dielectric processes.

Thirdly, methodologies for evaluating the V_{TH} instability during stress, generally called BTI, have been reviewed. First of all, a forward-reverse gate bias sweep is commonly used to evaluate the V_{TH} shift, which is a fast and easy method for lots-to-lots comparison. On the other hand, monitoring V_{TH} shift during a stress is more useful for understanding the time-dependent V_{TH} shift. Therefore, a standard V_{TH} shift characterization during a stress with the interruption of I_D-V_G characterization has been discussed, which will be applied in chapter 3. Furthermore, an eMSM technique is also reviewed towards a better understanding of bias temperature instability (BTI). This method includes a set of stress and recovery tests to evaluate trapping/de-trapping

dynamics with respect to the V_{TH} shift. This method is developed to collect the maximum stressed and relaxation information during one experiment, which will be applied in chapter 4 to understand the PBTI in fully recessed gate MIS-FET.

Chapter 3

Stability of D-mode AlGaN/GaN MIS-HEMTs on a 150mm Si substrate

3.1 Introduction

As already mentioned in chapter 1, conventional depletion-mode (D-mode) AlGaN/-GaN High Electron Mobility Transistors (HEMTs) employ a Schottky gate to switch ON/OFF the channel. Schottky gate HEMTs are limited in being biased in forward gate bias voltage due to high conductive gate current even under a low gate bias. Moreover, Schottky gate HEMTs often suffer high leakage current under an OFF-state. For power switching applications, AlGaN/GaN HEMTs need to have a large gate bias swing in order to switch quickly from an OFF-state (a large drain bias and a negative reverse gate bias) to an ON-state (a large forward gate bias). Therefore, AlGaN/GaN HEMTs have to maintain a low gate leakage current in both OFF-state and ON-state. To achieve such a low leakage current, a depletion-mode AlGaN/GaN MIS-HEMT with a bi-layer gate dielectric has been developed at imec [38]. The bi-layer gate stack consists of 10nm Si_3N_4 grown *in-situ* on top of the AlGaN/GaN epitaxial layer in the MOCVD reactor and 5nm Al_2O_3 deposited by Atomic-Layer-Deposition (ALD).

In order to provide a normally-off characteristic, D-mode GaN-based device is typically used in a normally-off cascode circuit, which is a D-mode GaN-based transistor in series with a low voltage E-mode Si MOSFET, as shown in Figure 3.1. In this circuit topology, the maximum gate voltage (V_G) in the GaN-based transistor is 0V in order to avoid the instabilities when the gate voltage is larger than 0V.

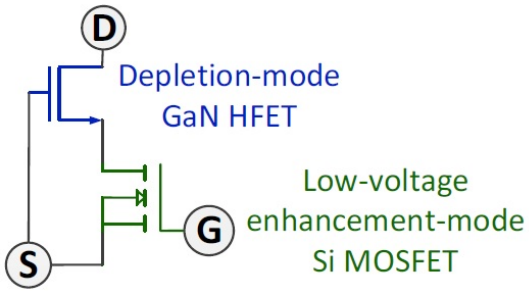

Figure 3.1: *Normally-off cascode switch circuit topology [102].*

However, in this chapter, this D-mode MIS-HEMT technology with a bi-layer is used to preliminarily investigate the dielectric behavior by means of a Time-Dependent Dielectric Breakdown (TDDB) and the stability of V_{TH} under a positive gate bias stress.

3.2 Device Description: AlGaN/GaN MIS-HEMTs with *in-situ* SiN/Al_2O_3

A schematic of the AlGaN/GaN MIS-HEMT is shown in Figure 3.2. This device is fabricated by using a Au-free CMOS-compatible process for AlGaN/GaN MIS-HEMTs. The double heterostructure epilayer (AlGaN/GaN/AlGaN) was grown by MOCVD and consists of a 200-nm AlN nucleation layer, a 2.3 μm $Al_{0.18}Ga_{0.82}N$ buffer layer, a 150 nm GaN channel, a 10 nm $Al_{0.25}Ga_{0.75}N$ barrier layer and a 10 nm *in-situ* grown SiN surface passivation layer. Then, 5 nm Al_2O_3 was deposited by ALD, followed by 120 nm high temperature low pressure chemical vapor deposited (LPCVD) nitride. The Ohmic contacts were formed by etching the triple dielectric stack with a low power SF_6 plasma, followed by Ti/Al/W deposition, dry etching of the metal stack and alloy at 600^{o}C. Before N-implant isolation, the Ohmic metal was capped by a patterned plasma enhanced chemical vapor deposited (PECVD) nitride. The gate was formed by selective removal of the LPCVD nitride in a SF_6 plasma using Al_2O_3 as etch stop layer, followed by deposition and dry etching of the W/Ti/Al gate metal stack. The process was completed by Al and Cu interconnect metallization layers.

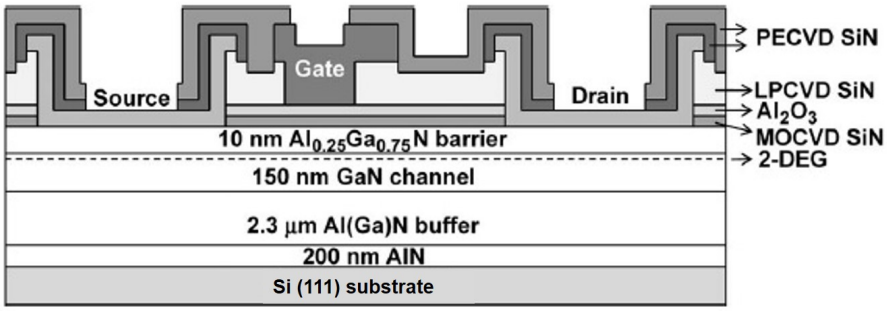

Figure 3.2: *Schematic diagram of the AlGaN/GaN MIS-HEMTs.*

3.3 Typical characteristics

Imec has extensively reported the characteristics of AlGaN/GaN MIS-HEMTs with *in-situ* SiN/Al_2O_3 for power switching applications [38]. Figure 3.3 shows the DC transfer characteristics for 10/5 nm SiN/Al_2O_3 as gate dielectric. The subthreshold slope is 80 mV/decade. The drain leakage and gate leakage in pinchoff is below 1×10^{-10} A/mm. The pulsed I_D–V_{DS} output current characteristics are shown in Figure 3.4.

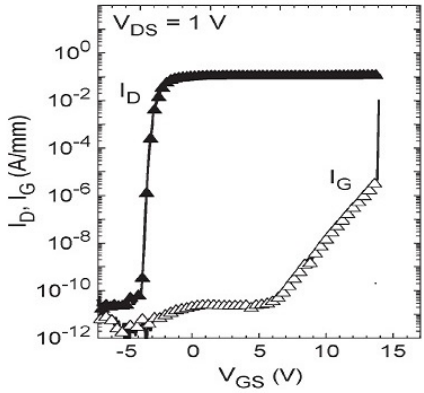

Figure 3.3: *DC characteristics (I_D and I_G versus V_{GS}) of a MIS-HEMT with a bi-layer gate dielectric (10 nm in-situ SiN and 5 nm ALD Al_2O_3) [38].*

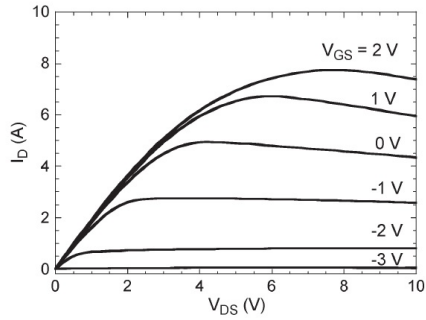

Figure 3.4: *Pulsed I_D–V_{DS} curves (pulse width, 1 ms) of a 20-mm-wide power transistor [38].*

Figure 3.5 shows the high-voltage OFF-state leakage. The OFF-state breakdown is larger than 600V. However, the OFF-state drain leakage curve shows the different behaviors in the different voltage ranges. For example, the drain leakage current increases fast below 50V. Then, the drain leakage current shows a slight decrease till $\sim$ 160V, further increasing again till 250V. Afterward, the drain leakage current shows a slight decrease again till $\sim$ 400V. In the end, the drain leakage current keeps increasing till the breakdown. These different behaviors are most probably due to the combination of lateral breakdown and vertical buffer breakdown. The different designs of the field plates [103] and different epitaxy layers [104] can improve the OFF-state breakdown as well as induce the different breakdown behaviors.

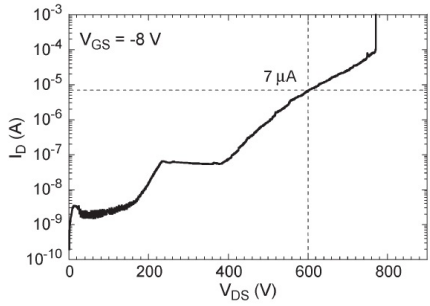

Figure 3.5: *High-voltage OFF-state drain leakage of a 20-mm-wide power transistor [38].*

3.4 Forward gate bias time-dependent dielectric breakdown (TDDB)

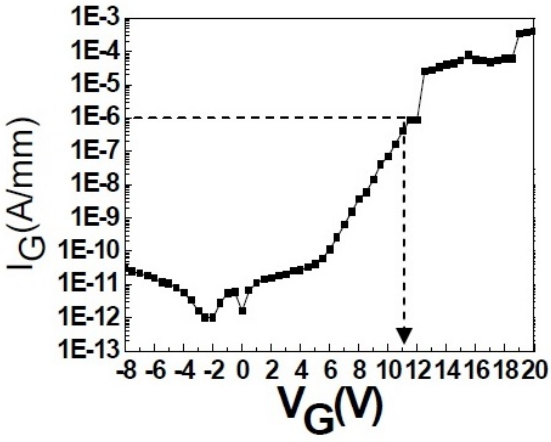

Figure 3.6: *Typical I_G–V_G characteristics of AlGaN/GaN MISHEMTs (sweeping rate: 1.5 V/s).*

The time-dependent dielectric breakdown (TDDB) methodology has been widely used to assess the gate degradation in CMOS technologies and has been successfully applied to evaluate the gate leakage current and extract the lifetime in GaN-based devices [79] under an OFF-state condition. In this paragraph, a forward gate TDDB methodology was performed in AlGaN/GaN MIS-HEMTs to assess the strength of the bi-layer dielectrics (10nm *in-situ* SiN and 5nm Al_2O_3). The test structures had the following dimensions: a gate length (L_G) of 1.5 μm, a gate-source distance (L_{GS}) of 2 μm, and a gate-drain distance (L_{GD}) of 2 μm. It should be noted that the gate width (W_G) of the test structures is 10 μm in order to test the dielectric intrinsic breakdown. The gate dielectric breakdown voltage is 11V (defined as the forward voltage for a gate leakage current of 1 μA/mm) as shown in Figure 3.6.

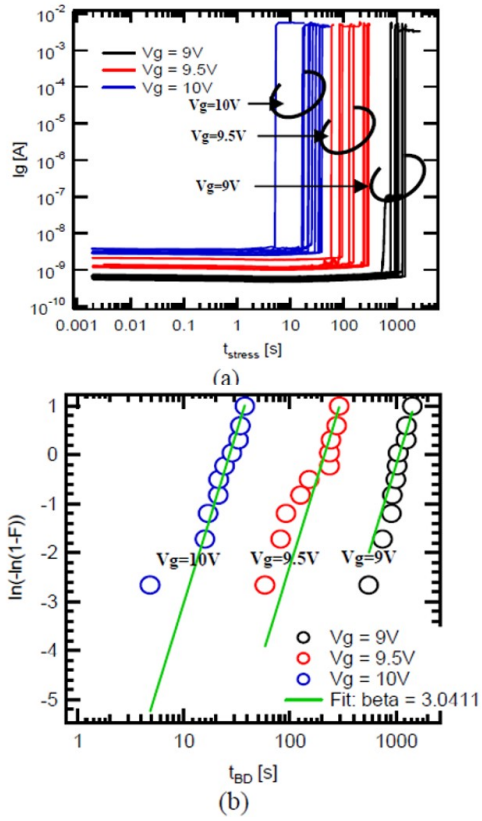

Figure 3.7: *(a) Gate current monitored on 30 devices subjected to TDDB experiments with three different gate voltages (10 devices per group). (b) Weibull plot of the time-to-breakdown (t_{BD}) distributions for the 3 TDDB gate voltage conditions (9V, 9.5V and 10V).*

In order to avoid extrapolation errors and to test the dielectric strength in the worst case scenario (highest temperature environment), the TDDB testing was performed at 200°C with V_G=10V, 9.5V and 9V for 10 devices for each stress condition (Figure 3.7 (a)). Similar to the TDDB evaluation in CMOS gate dielectrics [87], the time-to-breakdown (t_{BD}) of our devices is Weibull distributed (Figure 3.7 (b)). By fitting with a Weibull distribution, a large β = 3 is obtained (Figure 3.7 (b)), indicating a tight breakdown distribution and small variability. Moreover, according to Equation 2.7 and m = 0.35 - 0.4 [88], β = 3 could indicate that 7 $\sim$ 9 traps are needed to create the percolation path for the 15nm dielectric.

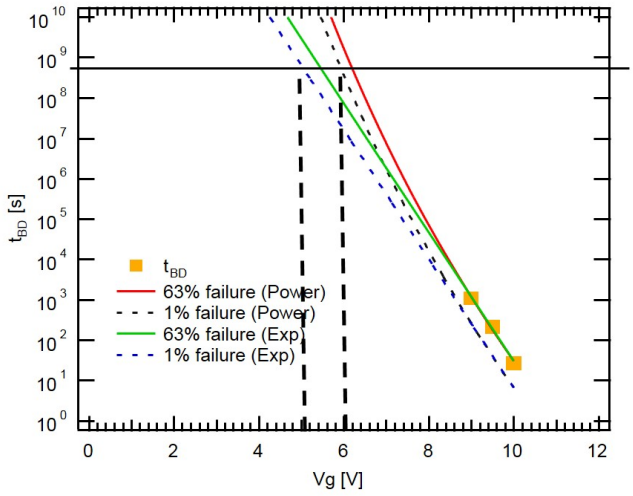

Figure 3.8: *Extrapolation of the t_{BD} at 200^{o}C towards the low bias conditions. After scaling to 1% at 20 years, an operating voltage of 5V or 6V can be determined by means of an exponential or a power law fitting, respectively.*

Figure 3.8 shows the lifetime extrapolation to 1% of failures by fitting the data with a power law or an exponential law for a gate voltage of 5V and 6V, respectively. This proves the excellent breakdown voltage strength and the 20-year lifetime of this dielectric at 200^{o}C.

3.5 Forward gate bias stress

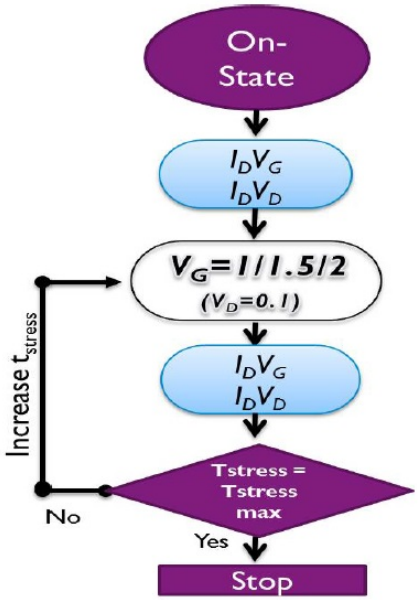

Figure 3.9: *Standard reliability testing procedure for the forward gate voltage stress.*

The ON-state stress testing flow is shown in Figure 3.9 and consists of the following steps: 1) A DC characterization is performed in order to characterize the fresh devices by measuring I_D–V_{GS} (V_{GS} is swept from -5.25V to 0V at V_{DS}=1V) and I_D–V_{DS} is swept from 0V to 5V at V_{GS}=0V). 2) Different ON-state stress conditions such as a forward gate bias voltage and a forward drain bias voltage are applied on the devices with a total duration of 15010 seconds. 3) The ON-state stress is paused at regular intervals for DC characterization (I_D–V_{GS} and I_D–V_{DS}). In order to avoid the artificial influences from the DC characterization, the sweep range of DC measurement is minimized and is performed to below 0V gate voltage to avoid possible trapping effects induced by a forward gate bias. The dimensions of the devices for the following tests are 1.5 μm, 2 μm, and 2 μm for L_G, L_{GD}, and L_{GS}, respectively.

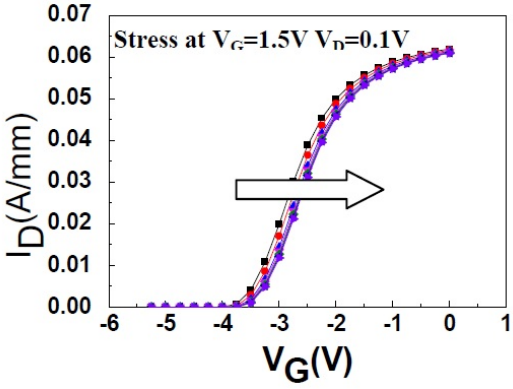

Figure 3.10: *Standard reliability testing procedure for the forward gate voltage stress.*

Forward gate voltage stresses of V_{GS}= 1V, 1.5V, and 2V were applied on 24 devices. Due to the limitation of the available stress time for the on-wafer characterization system, the total time was fixed at 15010 seconds and a fast DC characterization was monitored at a regular interval (10, 1010, 3010, 6010, 10010, and 15010 seconds). Figure 3.10 shows the I_D–V_{GS} characteristics during a stress.

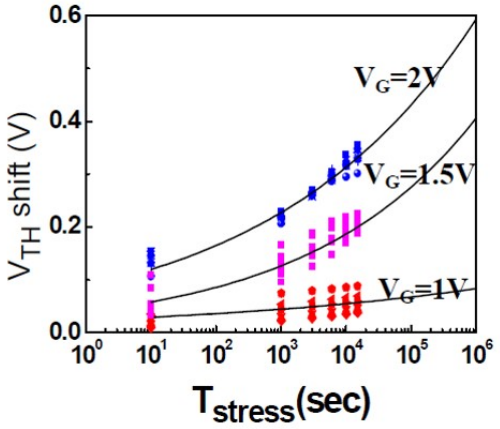

Figure 3.11: *V_{TH} shift versus stress time for 3 different gate voltages (8 devices per group).*

A positive V_{TH} shift is observed as the stress time is increased, showing a power law dependency of V_{TH} shift on the stress time, which has been commonly observed in

different technologies [98–101], and a V_{TH} shift is proportional to the applied gate stress voltage (Figure 3.11). The lifetime could be extrapolated by using a power law and the voltage shift after 20 years' stress time and time-to-0.5V V_{TH} shift with respect to three different gate voltages are shown in Figure 3.12 (a) and Figure 3.12 (b), respectively. We have calculated that a gate voltage of 1V, i.e. 5V gate overdrive with respect to V_{TH} which is around -4V, guarantees a 0.2V threshold voltage shift for a 20 years' stress time. This extrapolation has been performed by means of a power law fitting. These preliminary results indicate that the electron trapping by the interface state or the gate dielectric traps could lead to a V_{TH} shift under a positive gate bias. More dedicated and extensive studies will be discussed in the next chapter.

This study also indicates that these devices are suitable for applications in which the gate voltage operation condition does not exceed 1V, e.g. a normally-off cascode switching circuit, as mentioned before.

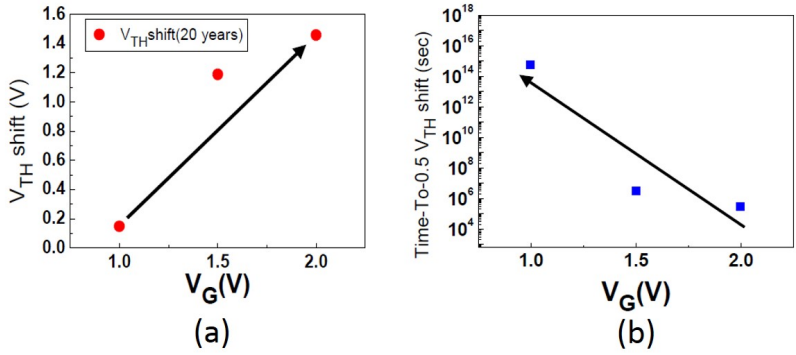

Figure 3.12: *V_{TH} shift for 20 years with different gate voltages (a) and Time-To-0.5V V_{TH} shift with different gate voltages (b).*

3.6 Summary of this chapter

Although a D-mode MIS-HEMT is used in a normally-off cascode, where the maximum gate bias is 0V, investigations of ON-state stress in terms of time dependent dielectric breakdown and the V_{TH} hysteresis have been reported in this chapter.

Firstly, the TDDB methodology is demonstrated to evaluate the gate dielectric strength under a forward gate bias stress, further estimating the lifetime towards a low percentage failures for 20 years. By employing a TDDB methodology at 200°C, the bi-layer dielectric has been proven to have an excellent dielectric strength. A gate voltage of

+5V or +6V for 1% of failures for 20 years lifetime can be extrapolated by using a power law or an exponential law, respectively. The comprehensive evaluation of TDDB in D-mode and E-mode transistors will be discussed in the next chapter in terms of different recessed depths, gate dielectric thickness, and gate width scaling.

Secondly, V_{TH} stability under a forward gate bias stress is studied. The results indicate that a forward gate voltage (V_G) bias stress induces a positive V_{TH} shift which is proportional to the applied gate forward voltage. This preliminary result points out that a positive V_{TH} shift under a forward gate bias stress could be due to electron trapping by the interface states under the gate dielectric or defects inside the gate dielectric. The detailed physical mechanisms will be discussed in the following chapter by evaluating the positive temperature instability (PBTI) and the interface state density (D_{it}) for the different gate dielectrics.

Chapter 4

Stability of E-mode recessed gate GaN MIS-FETs on a 200mm Si substrate

4.1 Introduction

In this chapter, the gate-related instabilities in E-mode recessed gate GaN MIS-FETs are studied in detail. First of all, in order to develop a high current E-mode transistor, the impact of the gate dielectric on the output drain current with respect to different recessed depths is studied. Secondly, in order to evaluate the strength of the gate dielectric in an E-mode transistor, the forward time-dependent dielectric breakdown (TDDB) evaluation is performed in D-mode and E-mode devices with different recess depths and different gate dielectric thicknesses. Thirdly, the origin of V_{TH} hysteresis, or PBTI (Positive Bias Temperature Instability), is studied by a dedicated set of stress-recovery tests (eMSM, as explained in chapter 2). Finally, a physical model is proposed to explain the PBTI in fully recessed gate MIS-FETs.

4.2 E-mode AlGaN/GaN transistors with the recessed gate process

4.2.1 GaN-on-Si epitaxy substrates in this study

All wafers were fabricated with a Au-free CMOS-compatible process on 200mm Czochralski-grown (111) Si wafers with a resistivity of 10Ωcm, starting with an AlN nucleation layer, a 2.3μm AlGaN buffer, a 150nm GaN channel, a 15nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 3nm GaN cap layer, which was used to avoid the oxidation of the AlGaN barrier. The epitaxy of the GaN cap/AlGaN/GaN stack was grown by means of metalorganic chemical vapor deposition (MOCVD) at a temperature of 1010°C with Trimethylgallium (TMGa), trimethylaluminum (TMAl), and Ammonia as precursors for Ga, Al, and N, respectively.

4.2.2 Recessed gate process and gate dielectrics used in this study

A recessed gate process is commonly used to reduce the 2DEG density under the gate, resulting in an E-mode characteristic for sufficiently deep recess, as already mentioned in chapter 1. At imec, the recessed gate is performed by the atomic layer etch (ALE) process, which has no selectivity between AlGaN and GaN. The ALE process is a two-step etching using separate oxygen (O_2) to oxidize AlGaN layer and boron trichloride (BCl_3) to remove the surface Al-GaN/GaN oxide [105] [106]. A 1.1nm etching depth per cycle can be precisely controlled by an ALE process. The typical surface roughness after an ALE process is about $0.2 \sim 0.25$nm in 1μm$\times 1\mu$m square, which is obtained by an AFM measurement (Figure 4.1).

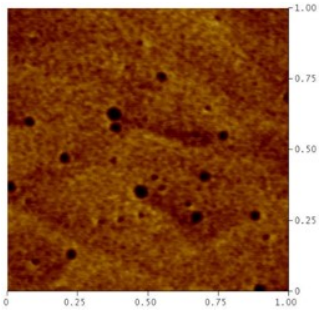

Figure 4.1: *AFM picture after an ALE process in the gate region.*

There are three different gate dielectrics used in this study.

1) RTCVD (Rapid Thermal Chemical Vapor Deposition) SiN: RTCVD SiN film (Si-rich) was deposited at 700°C with SiH_4 and NH_3 as precursors;

2) PEALD (Plasma-Enhanced Atomic Layer Deposition) SiN: PEALD SiN film (N-rich) was deposited at 300°C with SiH_4 and N_2 alternating cycles of SiH_4 and N_2 as precursors in an atomic layer deposition sequence. Based on the literature [62] [107], the initial N_2 plasma cycle provides a plasma nitridation of the (Al)GaN surface, thus providing the needed N-termination of the AlGaN surface;

3) ALD (Atomic Layer Deposition) Al_2O_3: ALD Al_2O_3 film was deposited at 300°C with TMA and H_2O as precursors.

The thickness of these dielectrics are varied and are stated in the following sections.

4.3 The impact of gate dielectric quality on the output drain current

In this section, two different gate dielectrics, i.e. RTCVD SiN and PE-ALD SiN, are both deposited in the recessed gate D-mode and E-mode transistors, as listed in Table 4.1. Note that -3.7nm in AlGaN barrier indicates 3.7nm etching depth into the GaN channel.

Table 4.1: *Summary of recessed depth and gate dielectric thickness in this study.*

Device	Recessed depth	Remaining AlGaN barrier	Gate dielectric thickness
D-mode MIS-HEMT	14.3nm	3.7nm	15nm
D-mode MIS-HEMT	16.5nm	1.5nm	25nm
E-mode MIS-FET	21.7nm	-3.7nm	25nm

4.3.1 Evaluation of the gate dielectric quality in recessed gate D-mode MIS-HEMTs

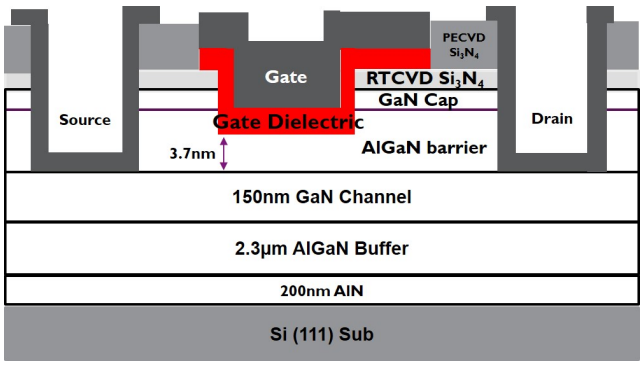

Figure 4.2: *Schematic cross-section of a D-mode recessed gate MIS-HEMT with 3.7nm remaining AlGaN barrier.*

The schematic of the device in this study is shown in Figure 4.2. A partial recessed gate process leads to a 3.7nm remaining AlGaN barrier, showing a D-mode characteristic. Two different gate dielectrics, i.e. RTCVD SiN (15nm) and PEALD SiN (15nm), were both deposited after a recessed gate process. Figure 4.3 shows the typical I_D-V_G

characteristics of devices with the two different gate dielectrics. The different V_{TH} values are most probably due to the different fixed charges brought by different gate dielectrics [108].

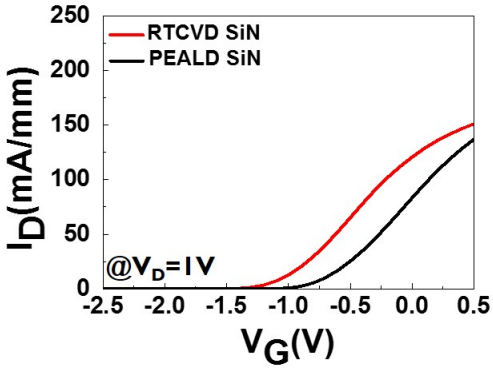

Figure 4.3: *I_D-V_G characteristics (linear-linear scale) of devices with different gate dielectrics.*

In order to understand the quality of the gate dielectrics and the interface properties between the gate dielectric and the AlGaN barrier, a frequency-dependent conductance analysis is done on a capacitor to extract the interface state density (D_{it}). A positive gate bias is needed to transfer the electrons from the channel to the interface between the AlGaN barrier and the gate dielectric to interact with the interface states, as shown in Figure 4.4. Therefore, the following conditions are measured on the capacitor structures: V_G=2.4V to 3.4V (RTCVD SiN) and V_G=3V to 4V (PEALD SiN). Note that the frequency-dependent conductance method assumes that the electrons interact with the interface states without considering the border traps [94].

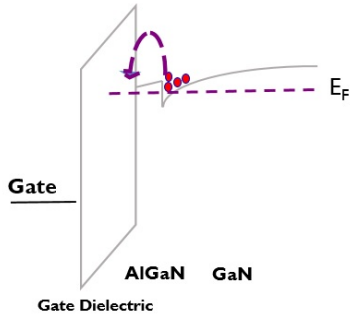

Figure 4.4: *The electrons could transfer across the AlGaN barrier to interact with the interface states under a positive gate bias.*

Figure 4.5 shows the extracted D_{it} values at the interface between the gate dielectric and the AlGaN barrier. The D_{it} is significantly lower for the device with a PEALD SiN ($D_{it}\sim 1\times10^{11}$–$2.3\times10^{12}cm^{-2}eV^{-1}$) gate dielectric than for the device with an RTCVD SiN ($D_{it}\sim 3.3\times10^{13}$–$3.5\times10^{13}cm^{-2}eV^{-1}$) gate dielectric.

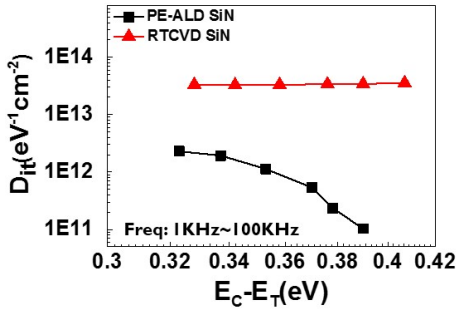

Figure 4.5: *D_{it} measurement of MIS-HEMTs with 3.7nm remaining AlGaN barrier on a capacitor. The trap state energy was estimated based on the Shockley–Read–Hall statistical model with a capture cross-section $1\times10^{-15}cm^2$.*

Furthermore, these devices are further characterized using the AC transconductance (AC-g_m) technique, as shown in Figure 4.6. The AC transconductance (AC-g_m) technique is developed to examine the effect of border traps on the carrier transport [109] [110], and it is assumed that the AC-g_m dispersion reflects the border trap density in the gate dielectric .

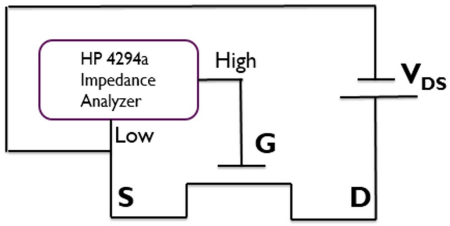

Figure 4.6: *Diagram of the AC-g_m measurement setup. A DC bias mixed with an AC sinusoidal signal (V_{rms}=20 mV) is applied on the gate while a small DC bias (50 mV) is applied on the drain to inject carriers across the channel.*

As shown in Figure 4.7, a significantly lower g_m peak dispersion is observed in the device with a PEALD SiN gate dielectric compared with the device with an RTCVD SiN gate dielectric. This suggests that the PE-ALD SiN has less border traps compared with the RTCVD SiN.

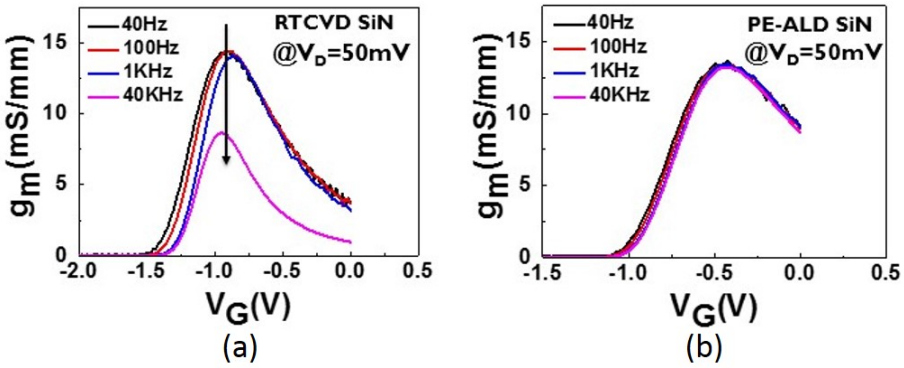

Figure 4.7: *G_m dispersion characteristics for 3.7nm remaining AlGaN barrier with an RTCVD SiN (a) and a PEALD SiN (b) gate dielectric.*

Figure 4.8 shows the typical I_D-V_G characteristics with a forward-reverse V_G sweep. The V_{TH} hysteresis is 1V and 0.3V in the device with the RTCVD SiN and PE-ALD SiN, respectively.

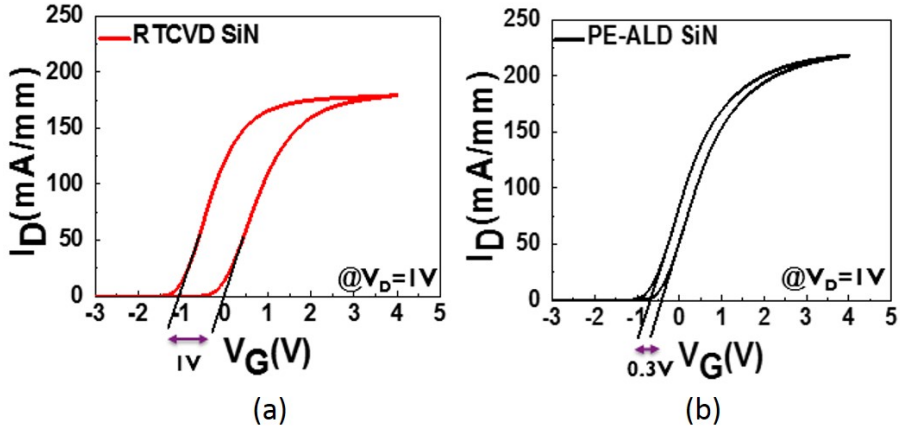

Figure 4.8: *I_D-V_G characteristics of the devices with 3.7nm remaining AlGaN barrier with an RTCVD SiN (V_{TH}= -1.3V) (a) and a PE-ALD SiN (V_{TH} = -1V) (b) gate dielectric.*

Therefore, a high correlation between V_{TH} hysteresis, D_{it}, and g_m peak dispersion, is observed. The device with a PEALD SiN shows a low D_{it}, small g_m peak dispersion, and low V_{TH} hysteresis. On the other hand, the device with a RTCVD SiN gate dielectric shows a high D_{it}, large g_m peak dispersion, and large V_{TH} hysteresis. This observation can be explained by the band diagram in the following.

As shown in Figure 4.9, under a positive gate voltage, the conduction band of the AlGaN barrier is pulled down. Based on the aforementioned characterizations, the electrons can be transferred from the channel to the interface between the gate dielectric and the AlGaN barrier, where they are trapped by interface states or border traps, leading to the V_{TH} hysteresis. Therefore, in order to minimize the hysteresis, a good dielectric quality with a lower D_{it} and less border traps is mandatory. The deposition of PEALD SiN is performed by alternating cycles of SiH_4 and N_2 plasma in an atomic layer deposition sequence [107]. The initial N_2 plasma cycle provides a plasma nitridation of the (Al)GaN surface, thus providing the needed N-termination to passivate Al or Ga dangling bonds.

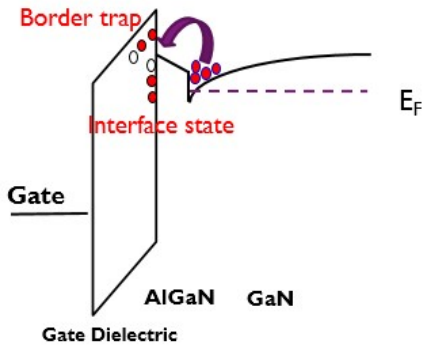

Figure 4.9: *Schematic band diagram indicating that electrons can be trapped by the interface states or the border traps under a positive gate bias condition.*

However, it is important to note that (1) the frequency conductance technique was originally developed to characterize interfaces with the physical assumption that the electrons only interact with the interface states [92] and (2) the AC transconductance (AC-g_m) technique was originally used to examine the effect of border traps on the carrier transport without considering the impact from the interface states [109]. However, such a high correlation between D_{it}, g_m peak dispersion, and V_{TH} hysteresis suggests that the D_{it} values from typical conductance measurements could be influenced by border traps, especially since a high positive gate bias is needed (more than 2V) to allow electrons to be injected across the AlGaN barrier and to interact with the gate dielectric interface in D-mode AlGaN/GaN MIS-HEMTs. On the other hand, the peak g_m dispersion could be affected by the interface states as well.

4.3.2 The impacts of gate dielectric quality on the output drain current in E-mode fully recessed gate MIS-FETs

After evaluating the gate dielectric properties as mentioned before, the sample with RTCVD SiN shows a high D_{it} and border trap density compared to the one with PEALD SiN. In order to understand the impacts of the gate dielectric on the performance of recessed gate E-mode MIS-FETs, these two gate dielectrics are deposited in the transistors with two different recessed depths, as shown in Figure 4.10.

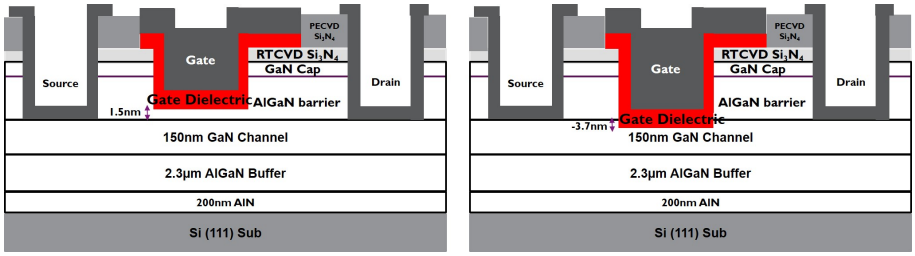

Figure 4.10: *Schematic cross-section of the E-mode recessed gate MIS-FETs with 1.5nm remaining AlGaN barrier (left) and 3.7nm etch depth into the GaN channel (right).*

Figure 4.11 shows the I_D-V_G characteristics and the transconductance (g_m) for devices with a 1.5nm remaining AlGaN barrier. When comparing the D-mode and E-mode devices, the device with an RTCVD SiN gate dielectric shows a more pronounced current drop and g_m degradation compared to the one with a PEALD SiN gate dielectric.

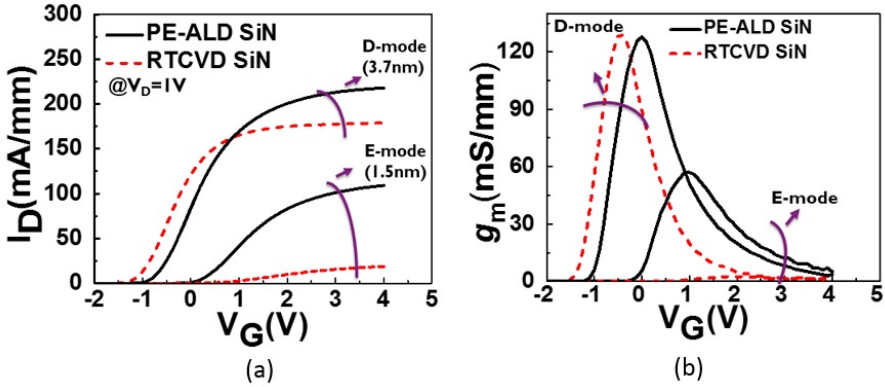

Figure 4.11: *I_D-V_G (a) and g_m-V_G (b) characteristics of the devices with 1.5nm and 3.7nm remaining AlGaN barrier. For the devices with a 1.5nm remaining AlGaN barrier, the V_{TH} is 0V (PEALD SiN) and 0.6V (RTCVD SiN). For the devices with a 3.7nm remaining AlGaN barrier, the V_{TH} is -1V (PE-ALD SiN) and -1.3V (RTCVD SiN).*

To increase the V_{TH}, the AlGaN barrier can be completely recessed into the GaN channel, resulting in an E-mode MIS-FET rather than a MIS-HEMT (Figure 4.10 (b)). Figure 4.12 shows the I_D-V_G and the g_m of the recessed gate MIS-FETs. The device

with an RTCVD SiN gate dielectric shows extremely lower current and g_m compared to the one with a PEALD SiN gate dielectric.

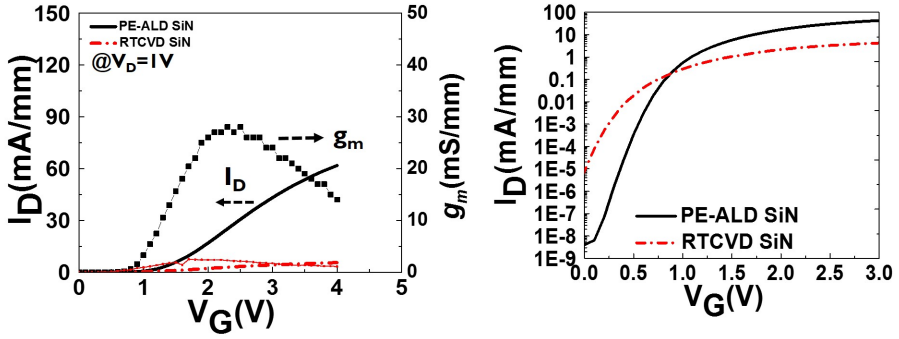

Figure 4.12: *I_D-V_G characteristics of the GaN-MISFET devices (left). I_D is below 10^{-8} mA/mm at V_G=0V (right). The V_{TH} is 1.1V and 1.3V, respectively for a PEALD SiN and an RTCVD SiN gate dielectric.*

Figure 4.13 and Figure 4.14 summarize how the I_D and g_m peak drop when the V_{TH} is increased. For a negative V_{TH} of -1V, both devices have similar current. However, the device with an RTCVD SiN gate dielectric shows a much more pronounced current drop and g_m degradation once the V_{TH} is above 0V.

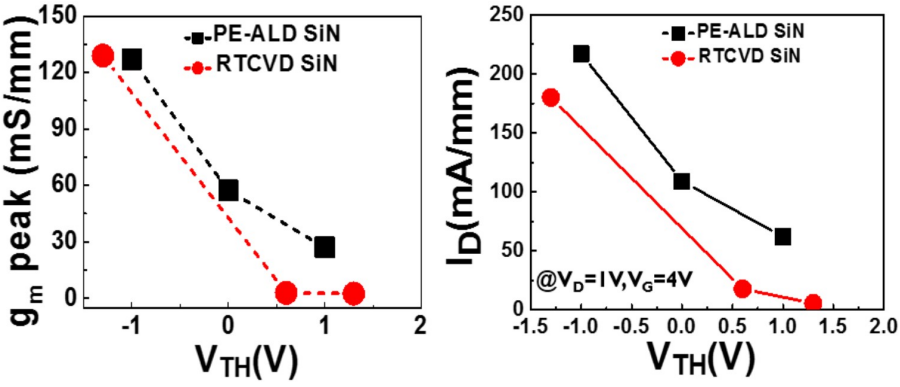

Figure 4.13: *g_m peak transconductance vs. V_{TH} (left) and I_D vs. V_{TH} (right) on devices with a PEALD SiN and an RTCVD SiN gate dielectric.*

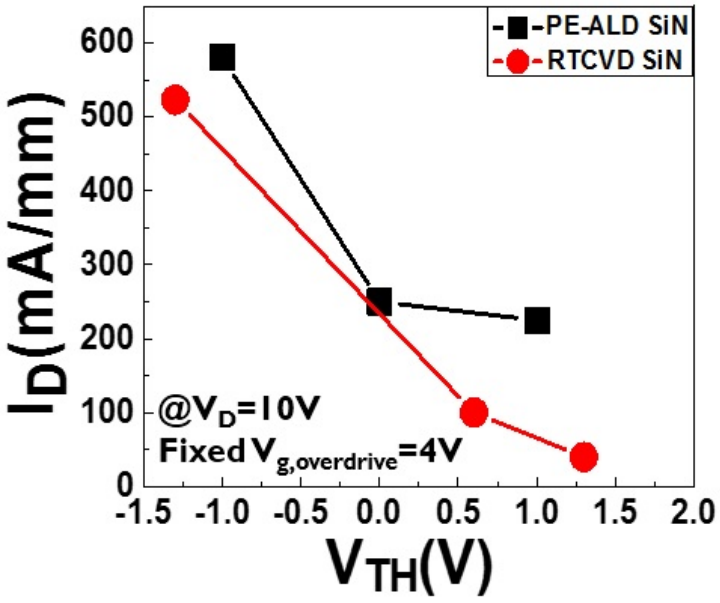

Figure 4.14: *I_D for a fixed gate overdrive of 4V and V_D=10V.*

Strongly or completely recessing the AlGaN barrier not only reduces the carrier concentration under the gate region but also brings the interface under the gate dielectric close to the channel (Figure 4.15). Indeed, g_m degradation could be either due to the change in carrier concentration or the change in carrier velocity [111]. However, the closer the traps to the GaN channel are, the stronger the electron scattering happens. So, such strong electron scattering could lead to serious mobility degradation, resulting in much more g_m degradation and current drop for the device with an RTCVD SiN gate dielectric. Yet, in a device with a better quality gate dielectric, i.e. a lower D_{it} or less border traps, the current drop can be lowered as shown in the I_D-V_D characteristics comparison of a fully recessed MIS-FET with a PEALD SiN and an RTCVD SiN (Figure 4.16) gate dielectric.

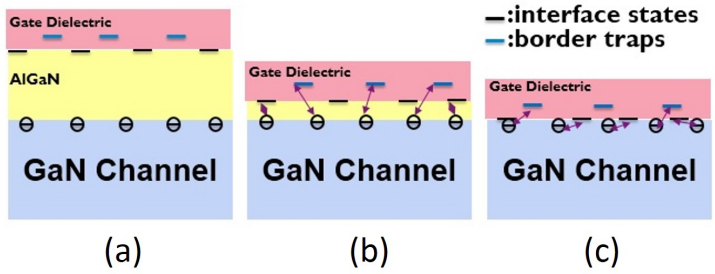

Figure 4.15: *For a poor quality gate dielectric, such as an RTCVD SiN, the electrons in the channel can easily be trapped by interface states or border traps. The closer these traps to the GaN channel are (a thinner AlGaN barrier is shown from (a) to (c)), the stronger the scattering happens. This results in serious g_m degradation and current drop (Figure 4.13 and Figure 4.14). However, this issue can be reduced by using a high quality gate dielectric, such as a PEALD SiN.*

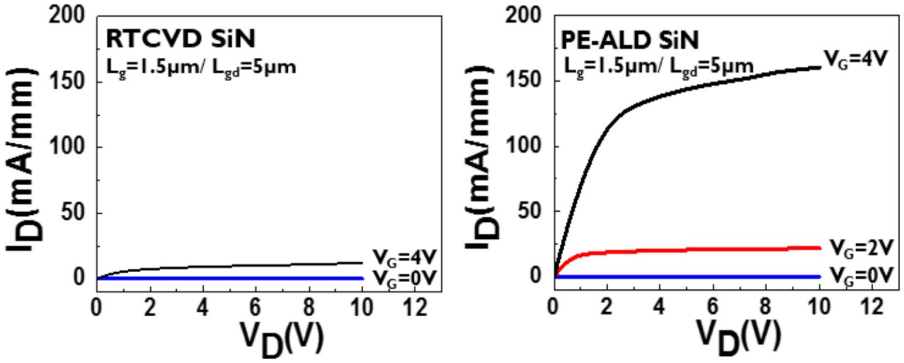

Figure 4.16: *I_D-V_D characteristics of the E-mode MIS-FETs with an RTCVD SiN gate dielectric (a) and a PE-ALD SiN gate dielectric (b).*

Conclusion

In summary, the impact of the interface properties and the quality of the gate dielectrics on the drain current characteristic of E-mode recessed gate MIS-FETs have been extensively investigated. The drain current reduction for a deep gate recess is observed. When the gate dielectric interface is very close to the GaN channel, the current is strongly reduced because of the increased scattering between the electrons and the

interface states/border traps, leading to g_m degradation, which is probably due to mobility degradation. However, this current drop can be lowered by using a good quality gate dielectric, which has lower D_{it} and less border traps.

4.4 Stability of forward gate bias time-dependent dielectric breakdown (TDDB)

As mentioned in chapter 1, AlGaN/GaN Metal Insulator Semiconductor High Electron Mobility Transistors (MIS-HEMTs) received significant attention because of their low gate leakage current, allowing a high forward gate bias. On typical CMOS technologies, the strength of the gate dielectric, especially time-dependent dielectric breakdown, is a critical reliability issue. So far, for GaN-based technologies, a TDDB evaluation has been successfully applied in Schottky gate AlGaN/GaN HEMTs to assess the gate degradation mechanism under a reverse bias [79]. Also, a forward gate bias TDDB evaluation has also been applied to D-mode MISHEMTs, as shown in chapter 3. Nevertheless, a comprehensive TDDB evaluation incorporating D-mode and E-mode transistors is lacking, especially the parameters affecting the gate dielectric strength in recessed gate AlGaN/GaN devices. In this section, forward TDDB measurements are performed in D-mode and E-mode AlGaN/GaN devices to assess the strength of the PEALD SiN gate dielectric (15nm or 25nm).

In order to understand the TDDB performance of D-mode and E-mode transistors, five different conditions for AlGaN barrier thicknesses are used in this study. The relevant parameters with respect to the recess depth, the thickness of the PEALD SiN gate dielectric, and the correlated V_{TH} values are shown in Table 4.2. Figure 4.17 shows the I_G-V_G characteristics of these different devices at 25°C and 150°C.

Table 4.2: *Summary of the important device parameters.*

Device	Recessed depth	AlGaN barrier	Gate dielectric thickness	V_{TH}
A (MIS-HEMT)	4.4nm	13.6nm	15nm	-4V
B (MIS-HEMT)	14.3nm	3.7nm	15nm	-1V
C (MIS-HEMT)	14.3nm	3.7nm	25nm	-2V
D (MIS-FET)	18.7nm	-0.7nm	25nm	0.3V
E (MIS-FET)	21.7nm	-3.7nm*	25nm	1.1V

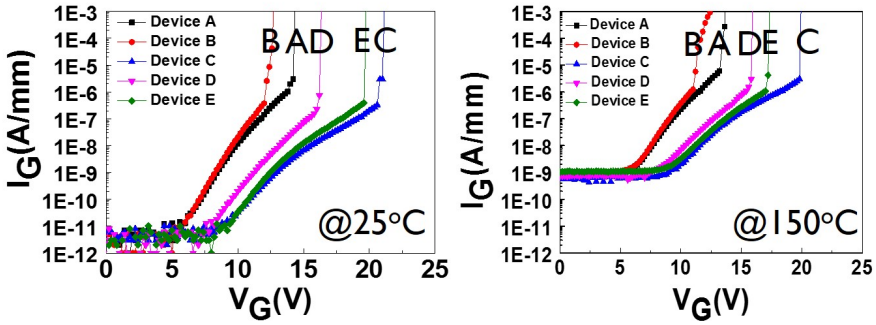

Figure 4.17: *I_G-V_G characteristics at 25°C and 150°C.*

The test structures have the following dimensions: a gate length (L_g) of 0.6μm, a gate-source distance (L_{gs}) of 2μm, and a gate-drain distance (L_{gd}) of 2μm. It should be noted that the gate width (W_g) of the test structures is 10μm in order to test the dielectric intrinsic breakdown. In order to avoid extrapolation errors and to test the dielectric strength in the worst case scenario (highest temperature environment), the TDDB testing is performed at 150°C. Three positive gate voltages are used at 150°C.

Figure 4.18 shows the gate current monitored during the TDDB experiments with three different gate voltages and the respective Weibull plots. Initially, the gate leakage gradually decreases. This could be due to the accumulated negative charges under the gate which suppress the gate leakage current. After a certain stress time, the gate leakage current becomes noisy. This is mainly attributed to the gradual formation of the percolation path. Once the percolation path has formed, the gate dielectric hard breakdown occurs, which shows a sudden increase of the gate leakage current. Based on the theory of the percolation path formation [87], t_{BD} is extracted from the time when the monitored current shows a step (Δ I) higher than 5×10^{-9}A. Then, the Weibull plot can be built based on the time-to-breakdown (t_{BD}) distributions for the three TDDB gate voltage conditions, as shown at the right side of Figure 4.18.

Since the first randomly generated percolation path in the gate dielectric statistically follows the Weibull distribution, as explained in chapter 2, the t_{BD} is calculated with the criteria of the first increase of the gate leakage current, e.g. 5×10^{-9}(A). In this case, the first initiation of the soft breakdown is considered to be this condition. From the device A to C, since there is a remaining AlGaN barrier under the gate dielectric, the first percolation path associated with the soft breakdown could be generated in the AlGaN barrier. Actually, the thickness of the epitaxy AlGaN barrier has $\pm$ 1nm non-uniformity. This could lead to a thin remaining AlGaN barrier under the gate in the Device D. Therefore, the soft breakdown we observed in the Device D could be a very thin remaining AlGaN barrier caused by a $\pm$ 1nm non-uniformity. The summary

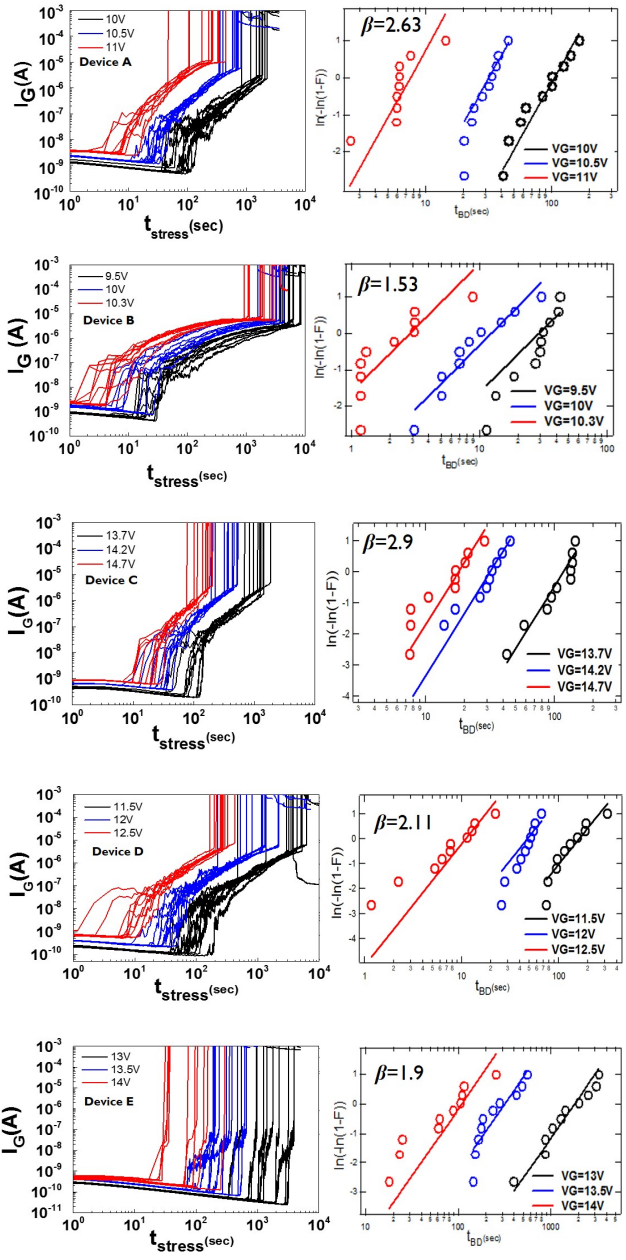

Figure 4.18: *TDDB gate current monitored on 30 devices with three different gate voltages (10 devices per group) at 150°C (left). Weibull plot of the time-to-breakdown (t_{BD}) distributions for the 3 TDDB gate voltage conditions (right). The small gate width (W_g=10μm) devices were used to study the intrinsic reliability.*

of the Weibull fitted parameter β (slope of the distribution) for the different recess depths and gate dielectric thicknesses is listed in Table 4.3 and is shown in Figure 4.19. A large β indicates a tight distribution and small variability. Recessing the gate leads to a smaller β, implying that the statistic distribution of t_{BD} becomes more spread. However, increasing the thickness of the gate dielectric strongly improves β (Device C) compared to the device with the same AlGaN thickness but thinner gate dielectric (Device B).

Table 4.3: *Summary of the correlated fitted β.*

Device	Fitted β
A(MIS-HEMT)	2.63
B(MIS-HEMT)	1.53
C(MIS-HEMT)	3.1
D(MIS-FET)	2.11
E(MIS-FET)	1.9

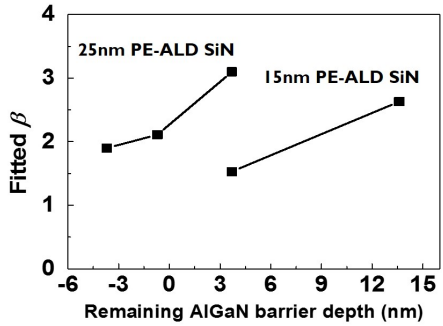

Figure 4.19: *Summary of the correlated fitted β in the function of recessed depths.*

Figure 4.20 shows the extrapolated V_G and the gate overdrive, i.e. extrapolated V_G - V_{TH}, versus remaining AlGaN barrier thickness, by fitting either with a power law or an exponential law under the condition of 0.01% failures of W_g=10μm after 20 years at 150°C. Considering the case of 15nm PE-ALD SiN, the extrapolated V_G is decreased as the remaining AlGaN barrier becomes thinner. Then, for a thick gate dielectric (25nm), the extrapolated V_G is higher again, as shown in Figure 4.20. Once the AlGaN barrier is completely etched, the extrapolated V_G is slightly decreased. However, the extrapolated V_G is increased to 8.2V (power law) or 6.8V (exponential law) when the etch depth is 3.7nm in the GaN. This is consistent with the three higher gate voltages

we needed to apply during the TDDB measurements of device E (Figure 4.18). In order to test the TDDB strength of the gate dielectric, the electrons have to be formed under the gate first in order to charge to the gate dielectric. Considering an enhancement mode transistor, i.e. Device E, the electron density under the gate is decided by the gate overdrive, i.e. V_G-V_{TH}. Therefore, a high V_{TH} needs a high V_G to form a certain amount of electron density under the gate dielectric. Therefore, compared with the Device D, the Device E needs three higher gate voltages for the TDDB experiments, leading to a higher extrapolated V_G shown in Figure 4.20. Therefore, Figure 4.20 (b) shows the the gate overdrive versus remaining AlGaN barrier thickness. In general, we can find that the gate overdrive is decreased when the remaining AlGaN barrier depth changes from 3.7nm to -3.7nm. This indicates that the high extrapolated V_G (Device E) could be most probably due to a high V_{TH}.

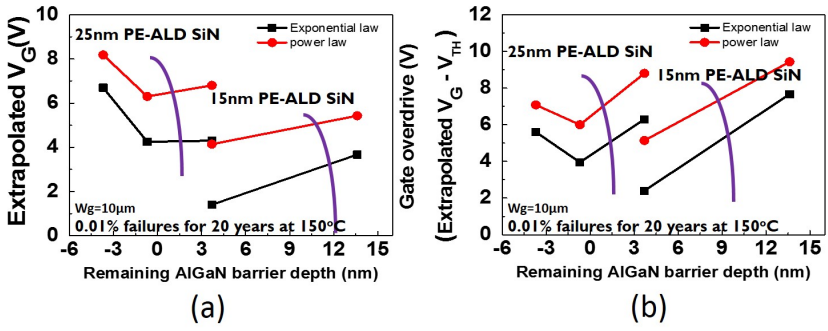

Figure 4.20: *Extrapolated V_G (a) and the gate overdrive (b) under the condition of 0.01% failures of W_g=10μm for 20 years at 150°C vs. remaining AlGaN barrier depth.*

4.4.1 Gate width scaling

In order to test the intrinsic gate dielectric strength, the device with small gate width has been evaluated and Figure 4.18 has shown that the t_{BD} data follows a Weibull distribution in the device with a small gate width (W_g). However, the possible influences of the extrinsic failures, e.g. process induced defects, weak spots, etc., cannot be excluded. This remaining issue can be answered by performing t_{BD} tests in devices with different gate area. In this section, the devices with fixed gate length and varying gate width are used.

Assuming that the breakdown spot occurs randomly in the gate area, a wide gate width device should statistically show faster t_{BD} data than a narrow gate width device. A wide device of width W_1 can be considered as the set of *n* smaller devices of width

W_2. Therefore, the probability to form a percolation path in the wider device is n times larger than in the narrower device. However, the failure distribution and β should remain the same since the nature of the failure should not be influenced by the device gate width. This can be elaborated mathematically [87] by considering the Weibull distribution as:

$$\eta_1 = \eta_2 (\frac{W_2}{W_1})^{1/\beta} \tag{4.1}$$

where η is the scale factor of the associated Weibull distributions.

Consequently, in the case of intrinsic failures, the Weibull distributions associated with failures in devices with width W_1 and W_2 should shift parallel and laterally with a factor of $(W_2/W_1)1/\beta$, as shown in the equation 4.1. Figure 4.21 shows the failure statistics of the devices with different gate width under the same gate bias. The Weibull distributions of t_{BD} are indeed laterally shifted when W_g (gate width) is increased. Moreover, when normalizing all of the data to a single width of 10μm, these data could be fitted with a single Weibull distribution (Figure 4.22). This proves that the device failure is intrinsic as it scales only with W_g, thus showing that breakdown spots are randomly distributed along the device width rather than being localized in one particular zone as in the case of extrinsic failures.

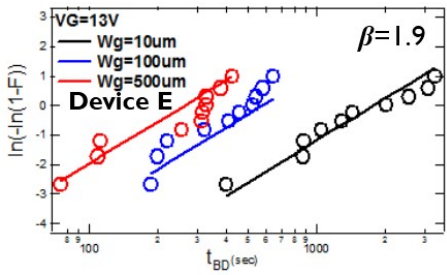

Figure 4.21: *Weibull plot of the time-to-breakdown (t_{BD}) distributions measured for V_G=13V in devices with different width (W_g=10μm, 100μm, and 500μm).*

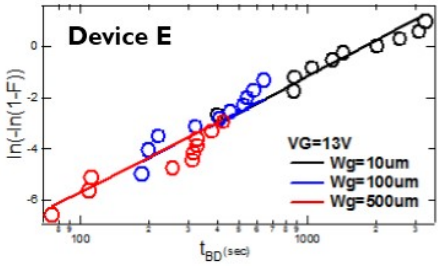

Figure 4.22: *Weibull plot of t_{BD} distributions measured for V_G = 13V for devices with different gate width (W_g =10μm, 100μm, and 500μm) normalized to 10μm gate width.*

4.4.2 Percolation path in fully recessed gate E-mode MIS-FETS

In the case of fully recessed gate MIS-FETs, since there is no remaining AlGaN barrier, the main percolation path is expected to form in the gate dielectric. Therefore, Device D and E should have the same β because β is proportional to the amount of traps to form the percolation path, as shown in equation 2.7 [87]. However, a smaller β in device E (β =1.9) compared with the Device D (β =2.11) was observed, indicating that a smaller amount of traps form the percolation path in device E. Figure 4.23 shows the TEM picture under the gate in device E, indicating that the gate dielectric around the side wall of AlGaN/GaN is thinner than the one on top of the GaN channel. Consequently, during the TDDB experiments, the percolation path could also form around the gate corner which has a thinner gate dielectric, resulting in a smaller β. This indicates that there could be a potential reliability issue in fully recessed gate E-mode MIS-FETs due to a thinner gate dielectric around the recessed gate corner.

4.4.3 Lifetime extrapolation in fully recessed gate E-mode MIS-FETS

Lifetime of 0.01% failures for the device with a large gate width, i.e. W_g=36mm can be predicted by either an exponential law or a power law. Figure 4.24 shows the lifetime extrapolation to 0.01% of failures for W_g=36mm at 150^{o}C. An operating voltage of 4.9V or 7.2V can be determined by means of an exponential law (solid line) or a power law (dash line) fitting, respectively. Regarding a high gate overdrive that is desired for E-mode devices, a gate dielectric of at least 25nm (or even thicker) are needed to achieve the required TDDB strength to guarantee a sufficient large gate overdrive.

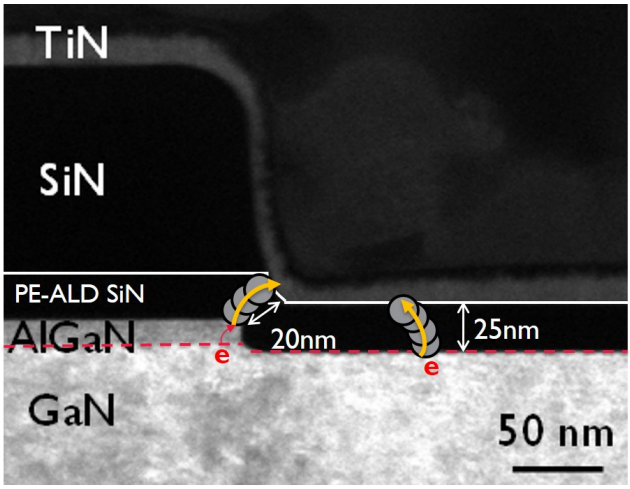

Figure 4.23: *TEM picture under the gate and schematic of possible percolation paths in fully recessed gate E-mode MISFETs.*

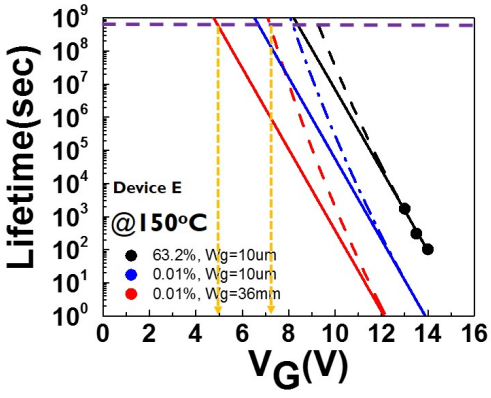

Figure 4.24: *Extrapolation of t_{BD} at 150°C towards low gate bias conditions.*

In addition to the PEALD SiN dielectric, it is also interesting to know the lifetime extrapolation in the fully recessed gate devices with an Al_2O_3 dielectric, which is the other promising gate dielectric in GaN-based devices. Figure 4.25 shows the lifetime extrapolation to 0.01% of failures for W_g=36mm at 150°C in the devices with an ALD Al_2O_3 gate dielectric. An operating voltage of 7.2V or 8.8V can be determined by

means of an exponential law (solid line) or a power law (dash line) fitting, respectively. This result indicates that 25nm of ALD Al_2O_3 gate dielectric can guarantee a sufficient TDDB margin.

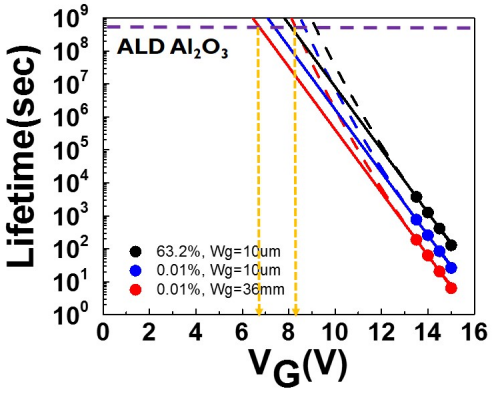

Figure 4.25: *Extrapolation of t_{BD} at 150°C towards low gate bias conditions in the device with ALD Al_2O_3.*

4.4.4 Conclusion

In this section, a forward bias gate TDDB evaluation in D-mode MIS-HEMTs and E-mode MIS-FETs with a PE-ALD SiN gate dielectric (15nm and 25nm thickness) has been extensively performed. First, the β of the Weibull distribution decreased for the device with a deeper recessed gate and the β increased for the device with a thicker gate dielectric. Secondly, for MIS-HEMTs, both for the power law and the exponential law, the extrapolated V_G (0.01% failures in the device with W_g=10μm after 20 years) is lower for a thinner AlGaN barrier under the gate. However, for MIS-FETs, the extrapolated V_G is larger for a deeper recessed gate. Thirdly, the Weibull distribution scales with different W_g. This proves that the gate dielectric breakdown mechanism is intrinsic along the gate width (W_g) direction. Fourthly, a deeper recessed gate could result in another percolation path around the gate corner because the gate dielectric is thinner on the sidewall, as observed in TEM inspection in Figure 4.23. This leads to a smaller β, i.e. less amount of the traps are needed to form the percolation path, in deeper recessed E-mode MIS-FETs. Finally, the lifetime is extrapolated to 0.01% of failures for W_g=36mm at 150°C after 20 years. In order to guarantee a gate overdrive (V_G-V_{TH}) with sufficient TDDB margin and to avoid the possible percolation path around a deep recessed gate corner, the PEALD SiN and ALD Al_2O_3 gate dielectrics require a minimum thickness of 25nm.

4.5 Towards Understanding Positive Bias Temperature Instability (PBTI) in fully recessed Gate GaN MIS-FETs

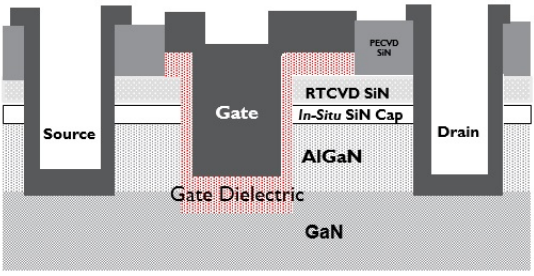

Figure 4.26: *Schematic of fully recessed gate GaN MIS-FETs.*

The V_{TH} shift has been observed in D-mode MIS-HEMTs, as shown in Figure 4.8. Such threshold voltage (V_{TH}) hysteresis after a positive forward-reverse gate sweep or V_{TH} shift during a positive gate bias stress, which is generally known as positive bias temperature instability (PBTI), has been reported for different gate dielectrics [112–118]. In order to develop technologically relevant solutions, it is necessary to gain in-depth understanding of the PBTI, especially E-mode devices. E-mode devices need a large positive gate overdrive, which could induce a serious PBTI. In this section, PBTI in E-mode fully recessed gate MIS-FETs, which have 3.7nm etching depth into the GaN channel, is studied in detail. The schematic of the studied device is shown in Figure 4.26 and Table 4.4 summarizes the gate dielectrics used in this study.

Table 4.4: Summary of the gate dielectrics used in this study.

Gate dielectric	Thickness
PEALD SiN	20nm
ALD Al_2O_3	25nm

4.5.1 I_D-V_G characteristics and interface characterization

The devices are first electrically tested by a positive forward-reverse gate I_D-V_G sweep (sweeping rate: 1.5V/s). Figure 4.27 shows the typical I_D-V_G characteristics after a

positive forward-reverse gate sweep. The V_{TH} hysteresis is 0.63V and 0.1V in the devices with PEALD SiN and Al_2O_3 gate dielectric, respectively. The Al_2O_3 gate dielectric shows a smaller V_{TH} shift compared to SiN gate dielectric. The V_{TH}'s are 0.7V and 0.1V, respectively, as calculated by the criterion of I_D=1mA/mm.

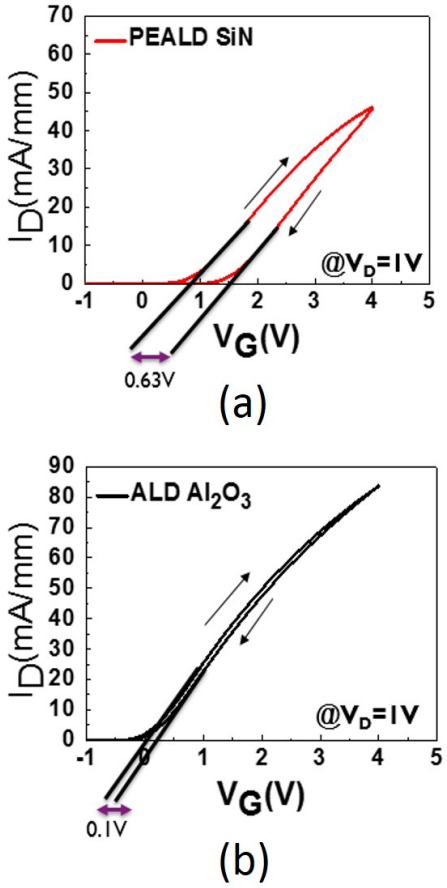

Figure 4.27: *I_D-V_G characteristics of the devices with a PEALD SiN (a) and ALD Al_2O_3 (b) gate dielectric. The V_{TH} hysteresis is 0.63V, and 0.1V, respectively. The V_{TH} and V_{TH} hysteresis were both calculated by the criterion of I_D=1mA/mm.*

Similar to literature [119–124], a standard frequency-dependent conductance analysis was performed first as the starting point to evaluate the gate stack quality when using these two dielectrics. Figure 4.28 shows the extracted D_{it} (interface state density) values by frequency-dependent conductance method at the interface under the gate

dielectric, which are $D_{it} \sim 5\times10^{12} - 4\times10^{11}$ $cm^{-2}eV^{-1}$ (PEALD SiN) and $D_{it} \sim 2\times10^{13} - 2\times10^{12}$ $cm^{-2}eV^{-1}$ (ALD Al_2O_3). The D_{it} are measured in the depletion region of the C-V measurements, where the gate bias is -0.3V $\sim$ 0.5V for ALD Al_2O_3 and 0.5V $\sim$ 1.0V for PEALD SiN, respectively. However, the impact of border traps on the extracted D_{it} values cannot be excluded [117]. Therefore, a more general analysis with a set of stress-recovery tests is used to understand the PBTI, as discussed in the following section.

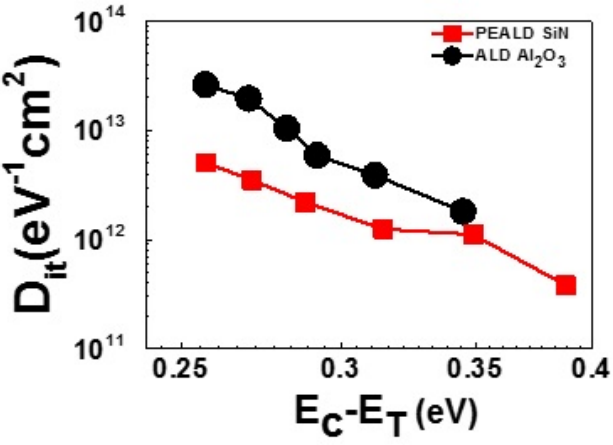

Figure 4.28: *D_{it} measurement in fully recessed gate MIS-FETs. The trap state energy was estimated based on the Shockley–Read–Hall statistical model with an assumed capture cross-section of 1×10^{-15} cm^2.*

4.5.2 Insight into PBTI mechanisms

In order to further understand the PBTI mechanism, a set of stress-recovery tests is conducted. A dedicated extended Measure-Stress-Measure (eMSM) sequence is performed. As mentioned in chapter 2, this measurement technique can capture several features of the PBTI kinetics after stress and recovery phases during a single experiment with a minimum sense delay of 1ms. In order to avoid pre-stressing the device during the initial I_D-V_G characterization sweep, the I_D-V_G is only measured up to the V_{TH} of the fresh device.

A non-linear power law dependence of ΔV_{TH} on t_{stress} is observed, as shown in Figure 4.29. Large $\Delta V_{TH} > 0.1$V is observed already at short stress time (2 seconds) and moderate gate stress voltages ($V_{ov,stress} = 0.4$V) (Fig. 4.29(a)) in the device with PEALD SiN gate dielectric. Similar to the BTI evolution in different device technologies

[98–101], ΔV_{TH} was also observed to follow a power-law of the stress time and stress overdrive voltage:

$$\Delta V_{TH} = A_0 (V_G - V_{TH0})^{\gamma} t_{stress}^{n} \tag{4.2}$$

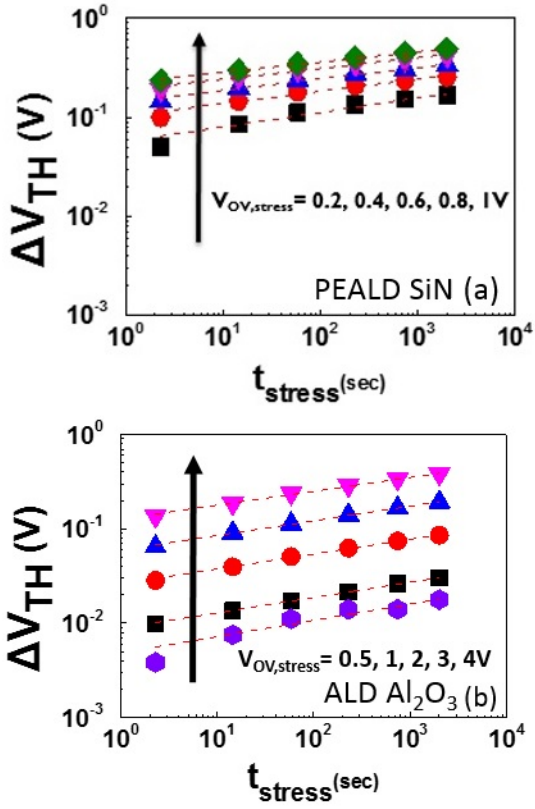

Figure 4.29: *ΔV_{TH} vs. t_{stress} in the device with a PEALD SiN (a) and ALD Al_2O_3 (b) in a logarithmic-logarithmic scale. Dashed lines are power law fits to the data, cf. equation 4.2.*

The time-dependence exponent *n* is estimated by fitting the power law (equation 4.2) to each experimental curve. Figure 4.30 shows the time exponent *n* vs. $V_{OV,stress}$, where $V_{OV,stress}$ represents the difference between a gate stress voltage and a threshold voltage (V_G-V_{TH}). In general, the time exponent *n* is in the range between $0.1 \sim 0.225$,

which is within the typical range of BTI reports in different technologies [98–101]. However, it is worth noting that the time exponent *n* of PEALD SiN decreases faster when increasing a gate voltage. The smaller exponent *n*, i.e. the weaker stress time dependency of the ΔV_{TH} evolution, indicates that a fast ΔV_{TH} has happened very quickly as soon as a stress voltage has been applied. On the other hand, in the device with ALD Al_2O_3, the time exponent *n* shows a slower decreases toward higher $V_{OV,stress}$.

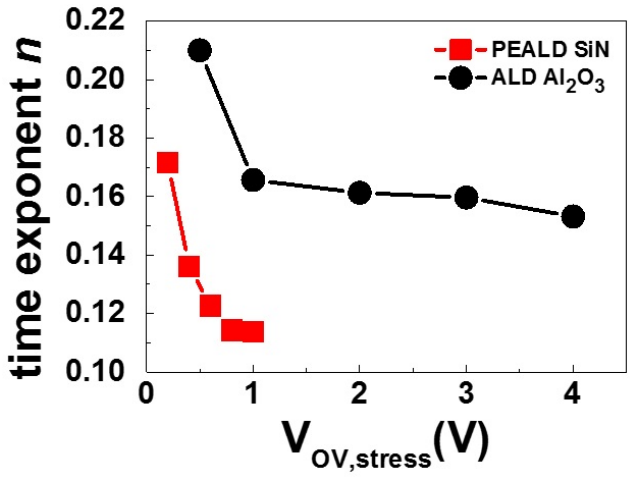

Figure 4.30: *Time exponent n with respect to the two different gate dielectrics.*

Furthermore, by extracting the ΔV_{TH} after a 2 second stress, the relationship of ΔV_{TH} and $V_{OV,stress}$ can be benchmarked, as shown in Figure 4.31. As one can clearly see, Al_2O_3 devices show $\sim$ 10 times lower ΔV_{TH} as compared to SiN. Moreover, a weak voltage dependence exponent $\gamma \sim 1$ is observed for PEALD SiN, while $\gamma \sim 2$ for ALD Al_2O_3. Note that γ describes the voltage dependency of ΔV_{TH}, as shown in the following equation:

$$\Delta V_{\mathrm{TH}} \propto V_{ov,stress}^{\gamma} \tag{4.3}$$

The physical origin of different γ values will be discussed in the following section.

The ΔV_{TH} during a stress can be expressed by using a semi-empirical acceleration model [101]:

$$\Delta V_{\mathrm{TH}} \propto A_0 exp(\frac{E_{\mathrm{A}}}{k_{\mathrm{B}}T})(\frac{V_{\mathrm{G}} - V_{\mathrm{TH0}}}{t_{\mathrm{OX}}})^{\gamma} t_{stress}^{n} \tag{4.4}$$

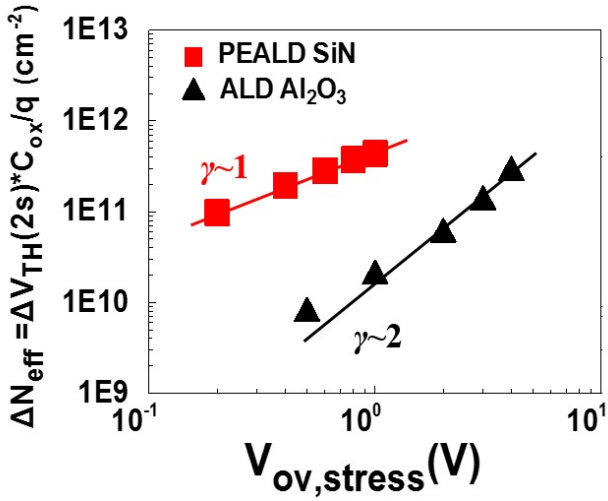

Figure 4.31: *PBTI shift benchmarking in terms of voltage dependency of* ΔV_{TH}.

This expression can be simplified as follows (Equation 4.5) once the same stress voltage is used.

$$\Delta V_{\mathrm{TH}} \approx A exp(-\frac{E_{\mathrm{A}}}{k_{\mathrm{B}}T}) t_{stress}^{n} \tag{4.5}$$

In order to estimate the mean activation energy of the charge capture process, one should consider the time necessary to reach a given V_{TH} (i.e. a given number of charged defects) at different temperatures, as shown in the following:

$$t_{stress} = \{\frac{\Delta V_{\mathrm{TH,given}}}{A exp(-\frac{E_{\mathrm{A}}}{k_{\mathrm{B}}T})}\}^{\frac{1}{n}} = \{\frac{\Delta V_{\mathrm{TH,given}}}{A}\}^{\frac{1}{n}} \{exp(\frac{E_{\mathrm{A}}}{k_{\mathrm{B}}T})\}^{\frac{1}{n}} \tag{4.6}$$

$$ln(t_{stress}) = \frac{1}{n} \cdot ln(\frac{\Delta V_{\mathrm{TH,given}}}{A}) + (\frac{1}{n}) \cdot E_A \cdot \frac{1}{k_B T} \tag{4.7}$$

Therefore,

$$< E_{A,capture} >= \frac{1}{n} \cdot E_A \tag{4.8}$$

From Eq. 4.8, the mean activation energy can be obtained by dividing the V_{TH} activation energy for *n*.

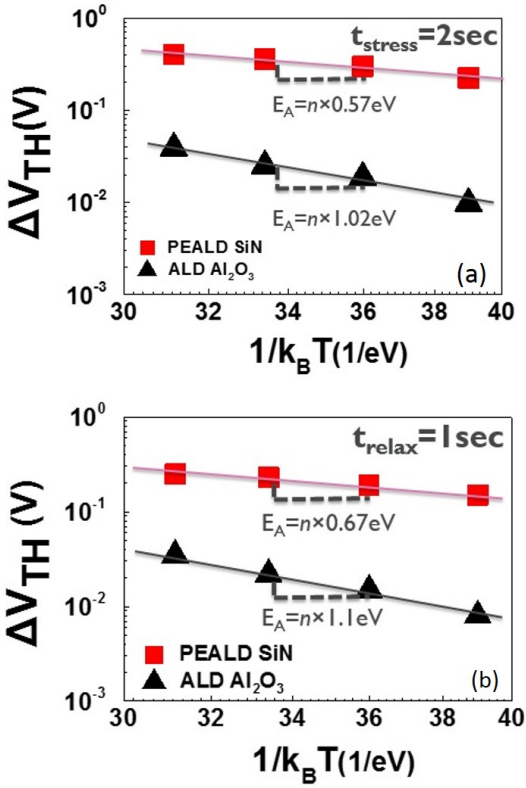

Figure 4.32: *Arrhenius plots of the V_{TH} measured during the stress (a) and relaxation (b) in devices with PEALD SiN and ALD Al_2O_3 gate dielectric. The ΔV_{TH} value were extrapolated when the devices were stressed at 1V of voltage overdrive for 2s and relaxed for 1s at different temperatures, i.e. 25°C, 50°C, 75°C, and 100°C. Similar E_A values are estimated for the emission process when ΔV_{TH} recovery is evaluated from 1ms to 1s after stress removal.*

Arrhenius plots of the temperature-dependence of the measured V_{TH} are shown in Figure 4.32 for the different devices. By fitting an exponential trend to the data, the V_{TH} activation energy can be estimated. The activation energy (after 2sec stress) is estimated to be 0.57eV and 1.02eV for the devices with PEALD SiN/ALD Al_2O_3 gate dielectric (time exponent *n* is 0.10/0.167), respectively. Furthermore, the activation energy (after 1sec relaxation) is estimated to be 0.67eV and 1.1eV for the devices with PEALD SiN/ALD Al_2O_3 gate dielectric, respectively. Please note that electron emission from traps back to the channel could happen during the 1ms delay (minimum delay) to estimate V_{TH} after stress removal. Since electron emission is also a thermally activated process, the estimated capture activation energy could be inaccurate. However, the large difference in the value of extracted E_A for the two dielectrics suggests different defect properties.

Another challenge to characterize PBTI is the partial recoverability once the stress is removed. This is often referred to as "relaxation". Such relaxation results in an underestimation of the PBTI degradation with standard delayed measurements. As the eMSM measurement sequence described previously, a set of relaxation curves in the device with PEALD SiN and ALD Al_2O_3 gate stack were collected, as shown in Figure 4.33. The relaxation transient is fitted with the empirical universal relaxation model [95] with the physical assumption of a recoverable (R) and permanent degradation (P) ascribed to different defect types [125], allowing an estimation for the fast V_{TH} component from the slowly-relaxing (or so-called permanent) component. While this distinction is only qualitative as it is based on an empirical model, it serves the purpose of further comparing the different PBTI behaviors of the two dielectrics. The V_{TH} recovery can be described as:

$$V_{\mathrm{TH}}(t_{\mathrm{stress}}, t_{\mathrm{relax}}) = R(t_{\mathrm{stress}}, t_{\mathrm{relax}} = 0) \times r(\eta) + P(t_{\mathrm{stress}}) \tag{4.9}$$

$$r(\eta) = \frac{1}{1 + B\eta^{\beta}} \tag{4.10}$$

where t_{stress} is the total stress time, t_{relax} is measured from the end of the last stress phase, and $\eta = t_{relax}/t_{stress}$ is the universal relaxation time; *B* is a scaling parameter. The functional form of Eq. 4.9 is similar to a stretched exponential, which is often used to describe relaxation of dispersive systems, and β has the attributes of a dispersion parameter. R (t_{stress}, t_{relax}= 0) represents a rough estimation of the "full" recoverable component extrapolated to t_{relax}= 0. Figure 4.33 shows typical set of PBTI relaxation traces and Figure 4.34 shows the recoverable (R) with respect to the different stress time and the permanent degradation (P). The ALD Al_2O_3 shows a smaller recoverable

component (R) even under a high stress gate voltage and a faster relaxation, as shown in Figure 4.33 (b). This can also be observed by looking at the ratio between the ΔV_{TH} of the ALD Al_2O_3 gate dielectric and the PEALD SiN gate dielectric as a function of the relaxation time (Figure 4.35). A faster dielectric defect discharge is clearly observed in the device with an Al_2O_3 gate dielectric. This faster relaxation suggests the electrons could be trapped shallower at the interface between the gate dielectric and GaN or inside the gate dielectric, inducing faster charge emission after stress removal. This could be due to a less favorable defect energy level with respect to the Fermi level in the GaN channel, which will be discussed in the following paragraph.

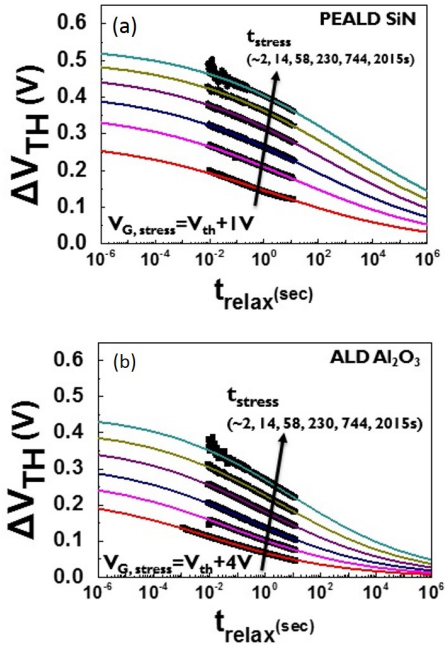

Figure 4.33: *Typical set of PBTI relaxation traces measured in the device with PEALD SiN (a) and ALD Al_2O_3 (b) gate dielectric. Note: different stress conditions (gate overdrive, stress time) were chosen in order to yield comparable degradation levels in the two different gate stacks. The lack of data at short relaxation times (<10ms) is due to the limited speed of the auto-ranging feature of the measurement instrument. B and β are 1.06 and 0.15 for the PEALD SiN and 2.72 and 0.18 for the ALD Al_2O_3, respectively.*

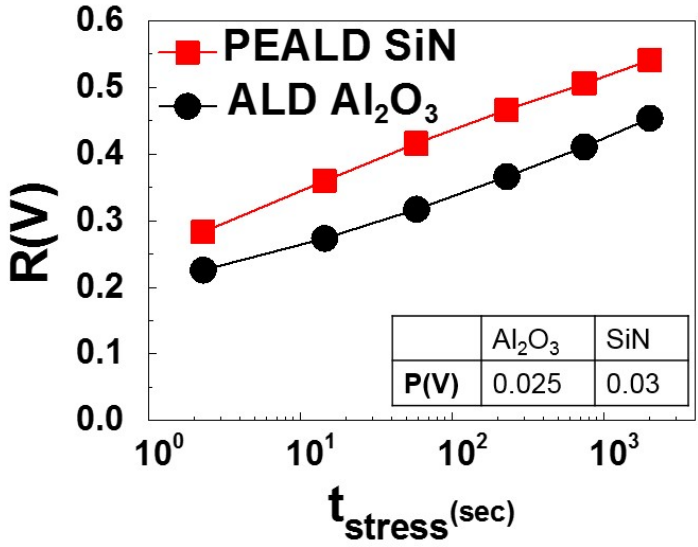

Figure 4.34: *The recoverable (R) with respect to the different stress time and the permanent degradation (P).*

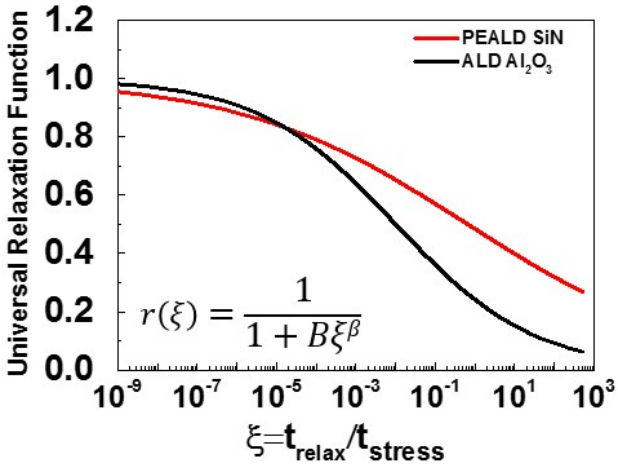

Figure 4.35: *The transients fitted with the universal relaxation model reveal faster relaxation for the device with Al_2O_3 gate dielectric.*

Although Al_2O_3 shows larger D_{it} levels (cf. Figure 4.28), the PBTI-induced V_{TH} shift is smaller compared to SiN. Recent literature shows that BTI in SiGe [99], Ge [100] [126], and InGaAs [98] [127] devices with high-k gate stacks is mainly caused by charging/discharging of defects inside the gate dielectric. A dielectric defect band based model has been used in literature to successfully describe BTI in various device technologies. Such model assumes the existence of a normal distribution of dielectric defect levels, and it ascribes BTI V_{TH} shifts to defect filling at varying gate voltages. For simplicity, the model assumes thermodynamic equilibrium, i.e. at each gate voltage all the defect levels above the channel Fermi level are considered empty, while all the levels below are considered filled. No kinetics is captured by this simplified model as it would require an accurate description of the lattice relaxation thermal barriers involved in the charging of each individual defect [128]. Therefore, the extracted defect density should be interpreted as representative of the given stress duration considered (i.e. larger density would be extracted for longer stress data). Note that, under the assumption of a voltage-independent power-law time exponent, i.e. time exponent *n* is independent of the stress voltage, longer stress time would only result in a rescaling of the fitted defect densities without modifying the defect energy profiles. Furthermore, a uniform distribution of defects along the dielectric thickness is assumed, and the applied gate voltage overdrive is assumed to drop solely on the gate dielectric, inducing a constant electric field. The impact of the possible presence of fixed charges is neglected. Figure 4.37 shows the experimental data of voltage dependency of ΔN_{eff} (effective trapped charge density = V_{THox}/q) against the calculated curves corresponding to the proposed defect band model. Note about the model calculation: the defect bands are modeled as a Gaussian distribution over energy as:

$$D_{ot}(E,x) = \frac{D_{ot0}}{\sigma_t\sqrt{2\pi}} exp\{ - \frac{E-\mu_t(x)}{2\sigma_t^2}\} \tag{4.11}$$

where E is the energy within the dielectric bandgap, μ_t and σ_t are the mean and the standard deviations of the Gaussian distributions and *x* is the spatial position inside the dielectric layer. Charged defects at different spatial positions also contribute differently to the total V_{TH} due to electrostatics. Moreover, an exponential decay term exp(-x/x_0) is included to account for the reduced tunneling probability of channel electrons toward defects located deeper in the gate dielectric (WKB approximation for tunneling probability). The characteristic tunneling distance x_0 was fitted as 1.4/2.54nm for Al_2O_3 and SiN, respectively. Note that using a Gaussian distribution of the defect levels is an assumption for the purpose to simplify the mathematical calculation of the model. Although different energy distributions of the defect might exist in reality, a similar result by shifting up the Fermi level energy in the channel would be obtained independently of the chosen distribution.

There are three fitting parameters, i.e. D_{ot}, μ_t, and σ_t, as shown in Equation 4.11. In order to describe the experimental data, we find that a defect distribution in Al_2O_3 centered $\mu_t \sim 1.15$eV (E_C + 1.15 eV) above the GaN conduction band with a relatively narrow energy spread ($\sigma \sim 0.42$eV) (Figure 4.36) and a defect distribution in SiN centered $\mu_t \sim 0.05$ eV below the conduction band (E_C - 0.05 eV) of GaN with a wide energy spread ($\sigma \sim 0.67$eV) (Figure 4.36) can nicely reproduce the experimental data (Figure 4.37).

Interestingly, the total volume density of dielectric defects (D_{ot}) in Al_2O_3 is $\sim$ three times larger than in SiN; however a large fraction of the defects in Al_2O_3 are not energetically favorable for channel electrons, and therefore they do not contribute to PBTI shifts at operating condition. On the contrary, the wide defect band in SiN is accessible for channel electrons already at low gate voltages, explaining the large V_{TH} shifts under a low gate bias and the weak voltage acceleration. These results also are qualitatively consistent with the different activation energies estimated (Figure 4.32). Namely, SiN gate dielectric has easily accessible dielectric defects, so the trapping mechanism of the SiN is accelerated less by the temperature, leading to a low activation energy (E_A=0.57eV) compared to the device with ALD Al_2O_3 (E_A=1.02eV).

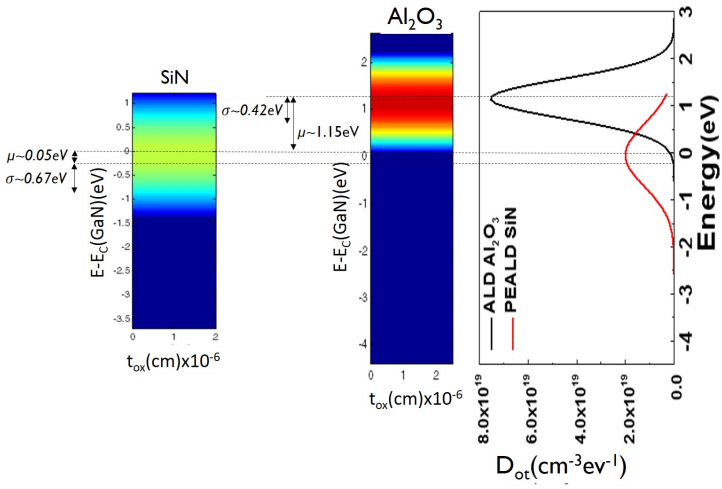

Figure 4.36: *Defect band models in the device with PEALD SiN gate dielectric and ALD Al_2O_3 gate dielectric (left) and the energy distribution of gate dielectric defects with respect to two different gate dielectrics (right).*

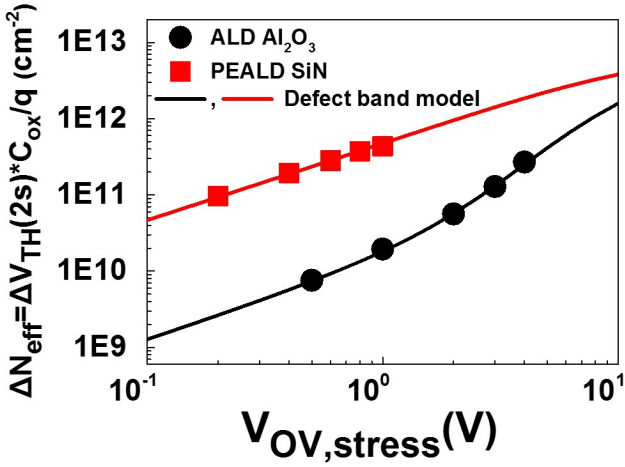

Figure 4.37: *The experimental data of ΔN_{eff} vs. voltage are excellently described by a defect band model calculation, as shown in Figure 4.36. The fitting parameters, including D_{ot}, μ_t, and σ_t, are shown in Figure 4.36.*

Note that, in the framework of the defect band model, the overdrive voltage dependency of ΔV_{TH} (γ in Figure 4.31), indicates the accessibility of dielectric defects in the gate dielectric, as illustrated in Figure 4.38. A low γ suggests the existence of a wide distribution of dielectric defects centered around the channel Fermi level, which can be easily accessed at low stress voltage. On the other hand, a high γ suggests a narrow distribution of defect level far away from the channel Fermi level. These physical mechanisms of PBTI in fully recessed gate GaN MIS-FETs are also consistent with the understanding of BTI in advanced gate stacks [129]. Based on all these observations, the Al_2O_3 gate dielectric is a much more promising to improve PBTI reliability than the SiN gate dielectric. It is worth mentioning that other gate dielectrics, such as HfO_2 and SiO_2, might have different dielectric defect distributions, resulting in further possibilities to improve PBTI.

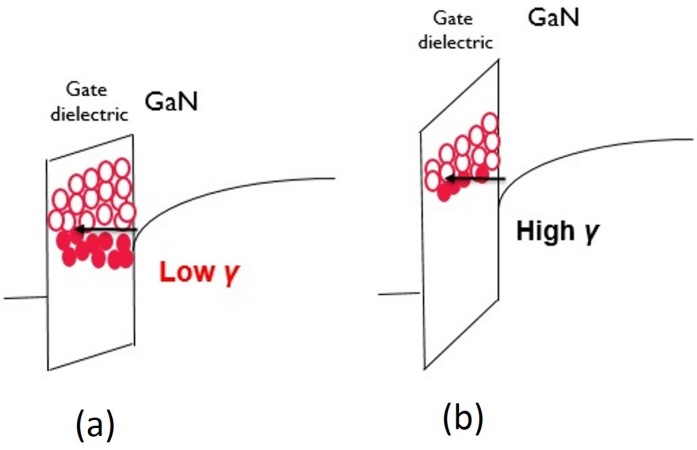

Figure 4.38: *Illustration of the relation between γ and defect distribution inside the gate dielectric. By comparing the PBTI shift benchmarking in Figure 4.31 with the defect band model in Figure 4.37, (a) a low γ (similar to the case of PEALD SiN) suggests the existence of a wide distribution of defect level centered around the channel Fermi level and (b) a high γ (similar to the case of ALD Al_2O_3) suggests a narrow distribution of defect level far away from the channel Fermi level.*

4.5.3 conclusion

The PBTI reliability of fully recessed-gate GaN MISFETs has been comprehensively investigated. By employing a dedicated set of stress-recovery experiments, i.e. the eMSM technique, PBTI has been characterized, highlighting the complex kinetics. The results indicate that: 1) V_{TH} evolution shows a power-law time dependence and 2) the PEALD SiN gate dielectric shows a low time exponent n, low voltage dependence of V_{TH} ($\gamma \sim 1$), and low capture activation energy (E_A = 0.57 eV), which can be explained by a defect band model we proposed to describe the experimental data. The PEALD SiN gate dielectric shows a wide defect band ($\sigma \sim 0.67$ eV) centered 0.05 eV below the conduction band (E_C - 0.05 eV) of GaN. In contrast, the defect distribution inside the ALD Al_2O_3 is 1.15 eV above the conduction band of GaN (E_C + 1.15 eV) and shows a narrower energy spread ($\sigma \sim 0.42$ eV). Therefore, the gate dielectric defects inside the PEALD SiN are much more easily accessible under a low gate voltage bias compared with ALD Al_2O_3 gate dielectric, indicating that the Al_2O_3 gate dielectric is more promising to improve the PBTI reliability. In sum, the distribution of defect energy levels inside the gate dielectric can contribute to the PBTI, which needs to be considered for further material and process optimization.

4.6 Summary of this chapter

In this chapter, the gate-related instabilities in terms of the impacts of the gate dielectric on the output drain current, forward gate bias time-dependent dielectric breakdown, and positive bias temperature instability (PBTI), in E-mode recessed gate GaN MIS-FETs have been discussed and strategies have been proposed to improve the devices' robustness under an ON-state condition. The key findings are summarized in the following.

First of all, the impact of the interface properties and the quality of the gate dielectrics on the output drain current has been investigated. Once the gate dielectric interface is approaching the GaN channel due to a recessed gate approach, the reduction of the output drain current has been observed.This is most probably because of the increased scattering between the electrons and the interface states/border traps, leading to g_m degradation, which is probably due to mobility degradation. However, this issue could be minimized by using a good quality gate dielectric, which has lower D_{it} and less border traps. Therefore, this study suggests that it is crucial to have a gate dielectric technology providing a lower D_{it} and less border traps to develop a high performance E-mode MIS-FET.

Secondly, the forward bias gate TDDB in D-mode MIS-HEMTs and E-mode MIS-FETs with a PE-ALD SiN gate dielectric (15nm and 25nm thickness) has been evaluated. The Weibull slope (β) of the Weibull distribution with respect to the different recessed depths have been shown and discussed. The β is decreased when the gate recess is deeper but is increased when the gate dielectric becomes thicker. Secondly, the extrapolated V_G regarding 0.01% failures in the device with W_g=10m after 20 years is lower for a thinner AlGaN barrier in MIS-HEMTs but larger in a deeper recessed gate MIS-FETs. Furthermore, the PE-ALD SiN gate dielectric requires a minimum thickness of 25nm to have a sufficient TDDB margin regarding 0.01% of failures for W_g=36mm at 150°C after 20 years. The 25nm ALD Al_2O_3 gate dielectric also shows sufficient TDDB margin regarding the same failure criteria.

Thirdly, by employing the eMSM technique, PBTI in E-mode recessed gate MIS-FET has been characterized. The defect band model is proposed to explain different PBTI characteristics in the devices with PEALD SiN and ALD Al_2O_3. Based on this model, the gate dielectric defects inside the PEALD SiN are much more easily accessible under a low gate voltage bias due to a wide defect band ($\sigma \sim 0.67$ eV) centered 0.05 eV below the conduction band (E_C - 0.05 eV) of GaN. On the other hand, the defect distribution inside the ALD Al_2O_3 is 1.15 eV away from the conduction band of GaN (E_C + 1.15 eV) and shows a narrower energy spread ($\sigma \sim 0.42$ eV). Therefore, the gate dielectric defect of Al_2O_3 can only be accessed under a high gate voltage. In sum, the distribution of defect energy levels inside the gate dielectric can contribute to the PBTI. For this reason, Al_2O_3 gate dielectric is more promising than SiN gate dielectric in

fully recessed gate GaN MIS-FETs.

Finally, the comparison of the PEALD SiN and ALD gate dielectrics in E-mode GaN MIS-FETs is shown in Table 4.5. Regarding the forward gate bias TDDB, PEALD SiN and ALD Al_2O_3 both have been demonstrated a sufficient TDDB margin with 25nm thickness regarding the 0.01% failures for 20 years at 150°C. However, ALD Al_2O_3 shows a better PBTI compared to SiN. It is worth noting that, however, ALD Al_2O_3 shows a lower V_{TH} compared to SiN. Therefore, none of these gate dielectrics can provide the advantages in combing a good PBTI and high V_{TH}, suggesting that further endeavors are needed to explore advanced gate dielectrics in using E-mode GaN MIS-FETs.

Table 4.5: *Comparison of PE-ALD SiN and ALD Al_2O_3 gate dielectrics in E-mode GaN MIS-FETs.*

Gate dielectric	TDDB	PBTI	V_{TH}
PE-ALD SiN	+	-	+
ALD Al_2O_3	+	+	-

Chapter 5

Stability of E-mode p-GaN AlGaN/GaN HEMTs on a 200mm Si substrate

5.1 Introduction

As mentioned in chapter 1, p-GaN AlGaN/GaN HEMTs are the other important architecture for E-mode power devices. This device concept is relative new and has been attracted more attention recently because an E-mode characteristic is able to be successfully realized and controlled. However, the reliability issues in such devices remain unknown. For example, the behavior of such devices under a large forward gate bias has not been explored yet. In this chapter, the forward gate breakdown mechanisms are explored and the physical mechanisms are proposed. Furthermore, preliminary high forward gate bias stresses are performed in order to understand the stability of V_{TH} and time-dependent p-GaN gate degradation.

5.2 Device Description

Figure 5.1 shows a schematic of p-GaN gate HEMTs. The devices were fabricated using a Au-free CMOS-compatible process. The AlGaN/GaN heterostructures were grown by MOCVD on 200mm Si (111) substrates. The layer stack consisted of a 2.4-μm-thick (Al)GaN buffer layer to enable high voltage operation, a 300 nm thick GaN channel layer and a 15 nm AlGaN barrier layer. The last top layer consisted of 70 nm M_g-doped p-GaN. The chemical Mg concentration was 1×10^{20}cm^3 and the active M_g concentration was 1×10^{18}cm^3, which corresponds to a 1% M_g activation rate. The TiN gate metal was evaporated on top of the p-GaN layer to form a Schottky contact. Then, a SiN hard mask was deposited on top of the TiN layer. Subsequently, a selective etch was performed till the AlGaN layer. Then, the SiN hard mask was removed and a SiN passivation layer was deposited. The p-GaN HEMT devices were further processed using Au-free process modules for Ohmic contacts and the various metal interconnect levels, including a thick power metal. Figure 5.1 shows a schematic

of the device up to the Ohmic contacts and a TEM inspection of the gate region. The devices with W_G=10μm, L_G=0.7μm, and L_{GD}=L_{GS}=0.75μm are used for this study.

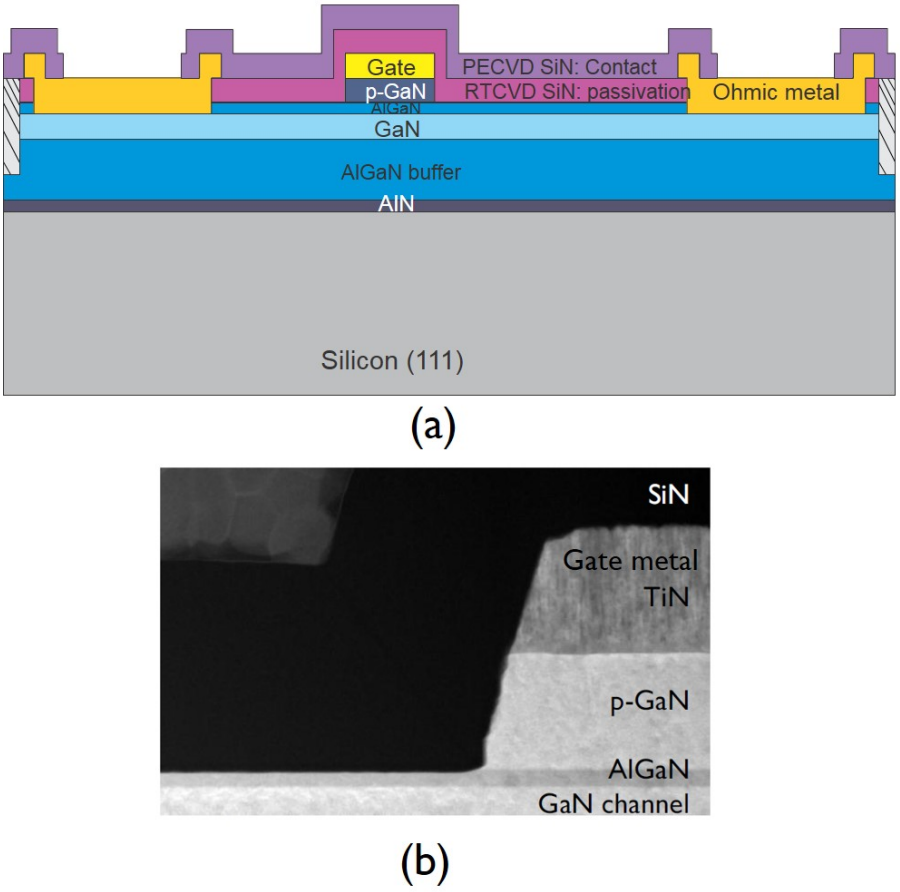

Figure 5.1: *Schematic cross-section of the Schottky metal/p-GaN gate AlGaN/GaN HEMT (a) and the TEM picture of the gate region (b).*

A typical I_D-V_G characteristic is shown in Figure 5.2. A threshold voltage (V_{TH}) of +1.6V is extracted by the maximum transconductance method. The output drain current (I_D) at V_G=8V and V_D=1V is 90mA/mm. The gate leakage current is below 5×10^{-7}mA/mm at V_G=8V. The subthreshold slope is 90mV/dec.

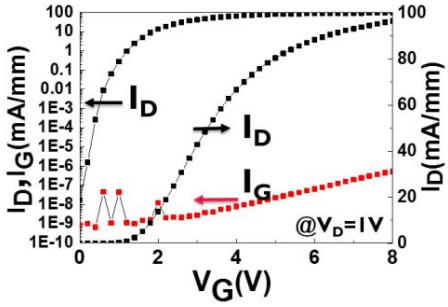

Figure 5.2: *I_D-V_G and I_G-V_G characteristics of p-GaN gate HEMTs.*

5.2.1 The forward gate bias breakdown mechanisms

In order to explore the forward gate breakdown mechanism, the I_G-V_G is measured at V_D=0V from 25°C to 200°C. The measurement flow is shown in Figure 5.3. All the experiments are done on fresh devices.

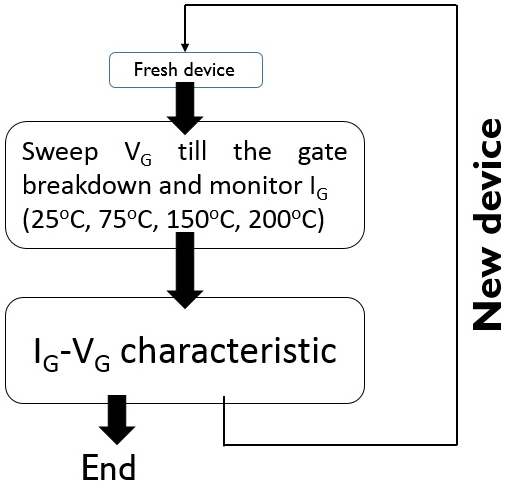

Figure 5.3: *Measurement procedure in this study.*

The I_G is monitored when the gate voltage is swept from 0V till the gate hard breakdown. An example of such an I_G-V_G characteristic is shown in Figure 5.4.

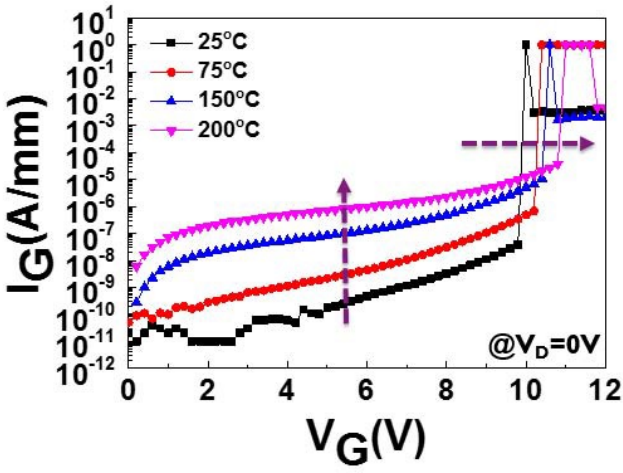

Figure 5.4: I_G-V_G *characteristics vs. different temperatures.*

Another fresh device is selected to repeat this experiment at a different temperature. A group of 15 devices with similar characteristics are measured at the same temperature and a total of 60 devices is used at four different temperatures. Before the hard breakdown occurred, the gate leakage current increases as the temperature increases. Furthermore, we observe that the gate breakdown increases as temperature increases. Figure 5.5 shows the summary of a statistical study of the gate breakdown measurements under each temperature condition. We can see that most of the gate breakdown values are tightly distributed around the average value. Furthermore, all of the data at 200°C are higher than at 25°C.

The positive temperature dependency of gate breakdown voltage ($+5\times10^{-3}$(°C/V)) is clearly observed, which is in contradiction to the temperature dependency of gate breakdown characteristic in AlGaN/GaN MIS-HEMTs [130] [131].

Positive temperature breakdown characteristics have been observed in Silicon CMOS technology [132] and depletion mode AlGaN/GaN HEMTs under an OFF-state bias [133], which are all explained by avalanche breakdown triggered by the impact ionization. Furthermore, GaN P-N diodes under a reversed bias also show this behavior [134–136]. This suggests that such a positive temperature forward gate breakdown characteristic in Schottky metal/ p-GaN gate AlGaN/GaN HEMTs could be related to avalanche breakdown as well. As shown in Figure 5.6, under equilibrium condition, the depletion region of the Schottky metal/p-GaN junction has a width of 50nm, which is estimated from a simulated Schottky junction with active M_g=1×10^{18}cm^3 and also can be simply calculated by using one-sided metal-semiconductor junction [132].

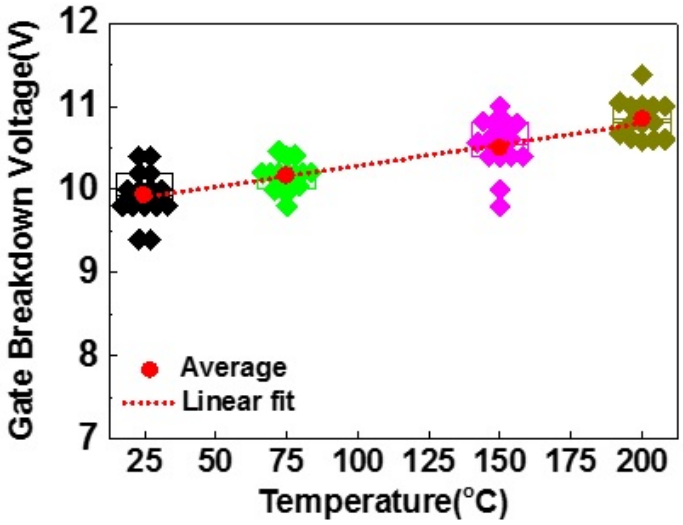

Figure 5.5: *The gate breakdown voltage vs. temperature. The gate breakdown voltage is extracted at 10^{-3}mA/mm gate leakage current. 15 devices are measured at the same temperature and a total of 60 devices is used at four different temperatures.*

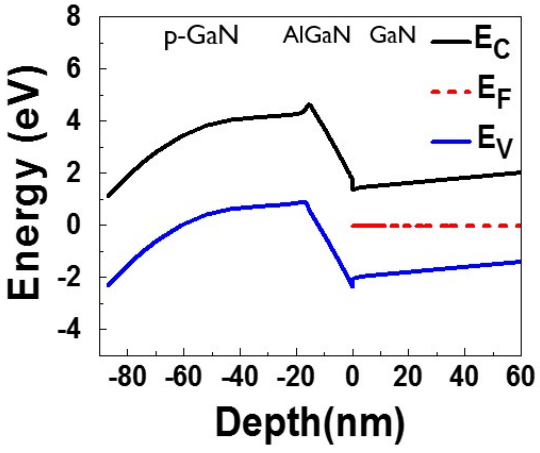

Figure 5.6: *Simulated band diagrams under an equilibrium condition.*

Furthermore, as shown in Figure 5.7, under a high forward gate bias condition, the

Schottky metal/ p-GaN diode is reversed bias, further extending the depletion region. Under a high forward gate bias, the electrons in the channel might be emitted over the AlGaN barrier and injected into the p-GaN layer. Once these electrons reach the depletion region, they are accelerated by the high electric field in the depletion region. The electric field is higher than 1.4MV/cm if a 70nm p-GaN layer has been assumed to be fully depleted to sustain the 10V of the gate breakdown voltage. The avalanche breakdown happens when the electrons move across the depletion region and acquire sufficient energy from the electrical field. Since the avalanche breakdown has a positive temperature coefficient, this mechanism can explain the observation, as shown in Figure 5.4 and Figure 5.5.

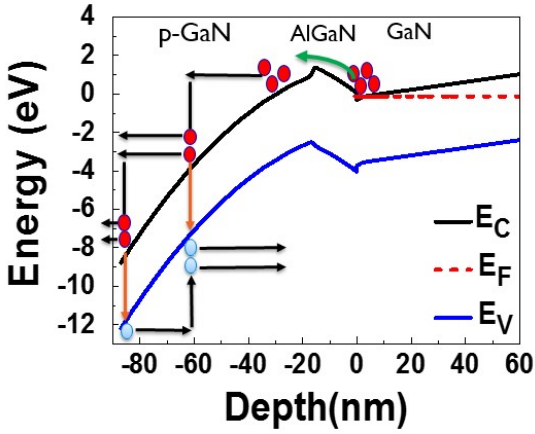

Figure 5.7: *Simulated band diagrams under a high gate voltage bias, e.g. V_G=10V.*

The electron and hole-related luminescence has been observed by Meneghini *et al.* on p-AlGaN gate HEMTs under a high drain bias with a moderate gate bias (V_G < 5.5V) [137]. They proposed that such kind of luminescence is due to the recombination of the holes injected from the gate and the electrons in the channel. In this case with p-GaN gate HEMTs, the emission microscopy measurements are carried out at different high gate biases before the gate hard breakdown occurs under the condition of V_D=0V. Note that the gate current is limited to 1μA during the measurement in order to test avalanche luminescence instead of the gate hard breakdown luminescence. The impact ionization is well known to induce the avalanche luminescence [136] due to the recombination of the electron-hole pairs. The light emission is clearly observed when the gate bias is close to gate hard breakdown (Figure 5.8 (a), 5.8 (b), and 5.8 (c)), proving that electrons can move across the space charge region, further generating the electron-hole pairs as mentioned before. Before the avalanche breakdown occurs, the electron-hole pairs have a chance to recombine again, yielding the light emission, as

shown in Figure 5.8 (d). However, the band-to-band recombination could also partially contribute to the light emission as well. Similar results have been observed in p-π-n GaN diodes [136], which is mainly due to M_g acceptor level in p-GaN region.

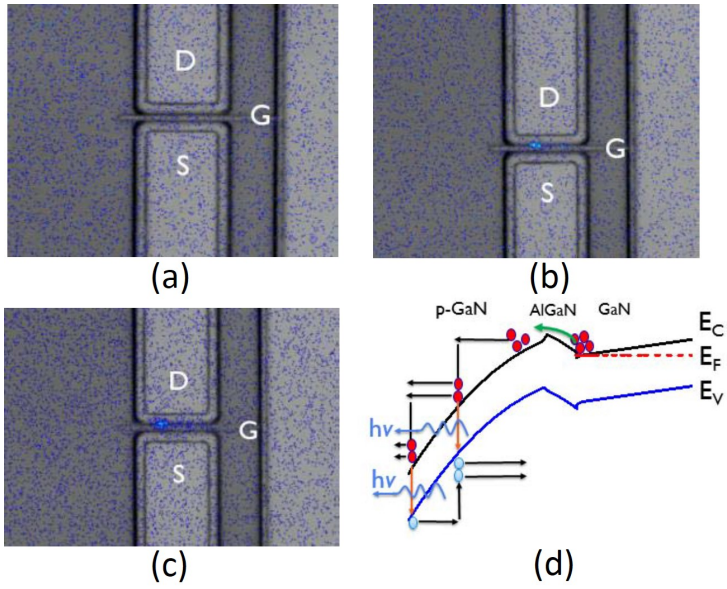

Figure 5.8: *EMMI measurement in p-GaN gate AlGaN/GaN HEMTs at V_G=9V (a), V_G=9.5V (b), and V_G=9.8V (c). The schematic of electron-hole recombination is shown in Figure 5.8 (d).*

5.2.2 Conclusion of the forward gate bias breakdown mechanisms

In this section, the forward bias gate breakdown mechanism in Schottky metal/p-GaN gate AlGaN/GaN HEMTs has been studied. First, the positive temperature dependency of the gate breakdown voltage is clearly observed ($+5\times10^{-3}$°C/V). The average gate breakdown voltage at 200°C is +1V higher than the one at 25°C. Such a gate breakdown phenomenon can be explained by avalanche multiplication in the depletion region of the Schottky metal/p-GaN junction. Once the electrons transfer to the p-GaN region, they can be accelerated by a high electrical field in the depletion region, yielding impact ionization. Finally, an avalanche luminescence is observed by means of EMMI measurement, proving that electron-hole pairs could indeed be generated under a high V_G bias.

5.2.3 The high forward gate bias stress in p-GaN AlGaN/GaN HEMTs

In this section, a preliminary set of tests is conducted to investigate the device's degradation. Three different gate biases, i.e. V_G=9V, V_G=9.5V, and V_G=10V, are used to stress the devices with a total duration of 4110 seconds. The I_D-V_G and I_G-V_G characterizations are performed after 10s, 110s, 610s, 1110s, etc., to investigate the device's characteristics.

Figure 5.9 shows the I_D-V_G characteristics during a V_G=9V stress.

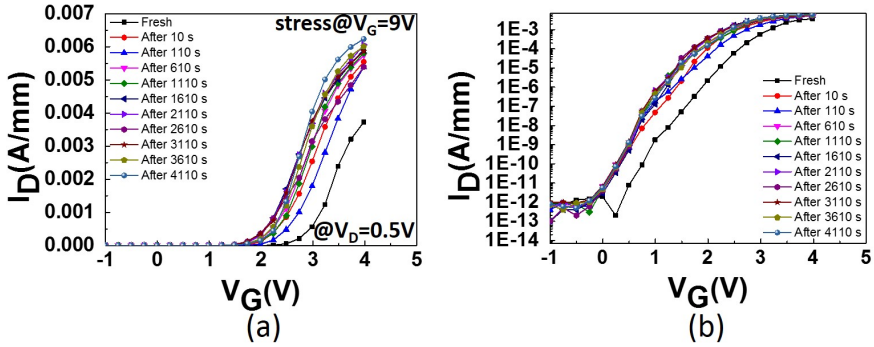

Figure 5.9: *I_D-V_G characteristics in a linear-linear scale (a) and a logarithmic-linear scale (b).*

Figure 5.10 summarizes the V_{TH} shift versus the stress time. The V_{TH} is calculated by the criterion of I_D=1mA/mm. Unlike a typical positive V_{TH} shift observed in MIS-HEMTs (chapter 3 and 4), the V_{TH} generally shifts in a negative way during a stress at V_G=9V. The V_{TH} shift $\sim$ -0.6V is observed after a 10s stress. However, a slight recovery is observed after a 110s stress. This recovery could be ascribed to a faster relaxation when a stress is removed or the impact of the I_D-V_G characterizations. Afterward, a further negative shift is observed when the device is stressed for a longer time.

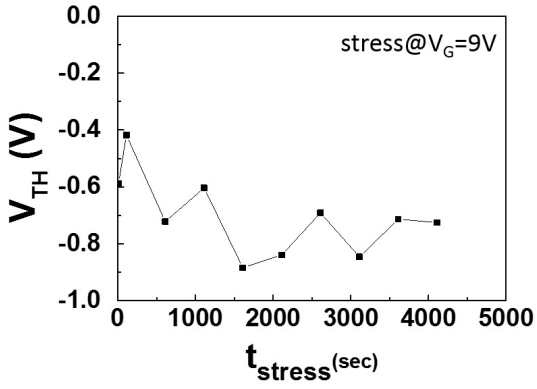

Figure 5.10: *V_{TH} shift in the function of the stress time during a stress at V_G=9V.*

A certain amount of hole concentration exists in the p-GaN region due to the doping with M_g and more and more holes could be created due to impact ionization, as mentioned before. Under a positive V_G, these holes could be injected to the AlGaN barrier or even GaN channel [51] [137] [138]. Such hole movement could explain the negative V_{TH} shift under a positive gate bias, as shown in Figure 5.11. These holes could be trapped by the interface states at the interface between p-GaN and AlGaN layer and by the bulk defects in the AlGaN layer. In order to maintain the charge neutrality, more holes at the interface between p-GaN and AlGaN induce more electrons in the channel, further leading to the negative V_{TH} shift.

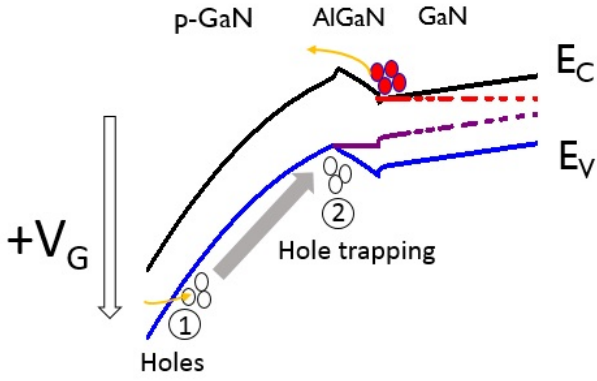

Figure 5.11: *Schematic of the hole trapping under a positive gate bias.*

In addition, I_G is monitored during a stress at V_G=9V. Figure 5.12 shows I_G during this stress. After a certain stress time ($\sim$ 30 sec), the current becomes noisy, indicating that there is degradation. However, time-dependent p-GaN gate breakdown is not observed during this stress.

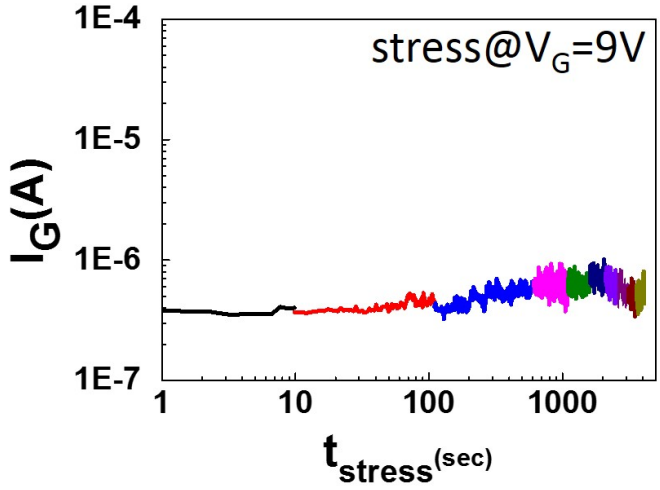

Figure 5.12: *Monitored I_G during a stress of V_G=9V.*

Furthermore, the device is stressed under higher gate biases, e.g. V_G=9.5V and V_G=10V. Figure 5.13 shows the I_D-V_G characteristics during the stress of V_G=9.5. A negative shift of the I_D-V_G characteristic can be observed. However, time-dependent p-GaN gate breakdown is observed after $\sim$ 717s, as shown in Figure 5.14. After a p-GaN gate hard breakdown occurred, the drop of the I_D at V_G=4V and the increase of I_D at V_G=-1 are observed.

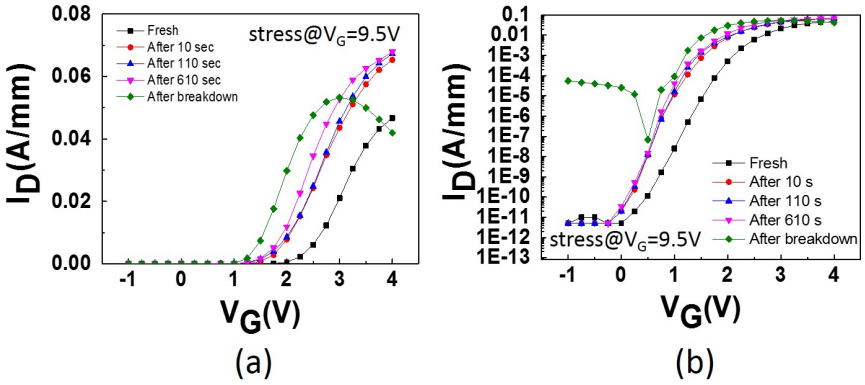

Figure 5.13: *I_D-V_G characteristics during the stress of V_G=9.5V in a linear-linear scale (a) and a logarithmic-linear scale (b).*

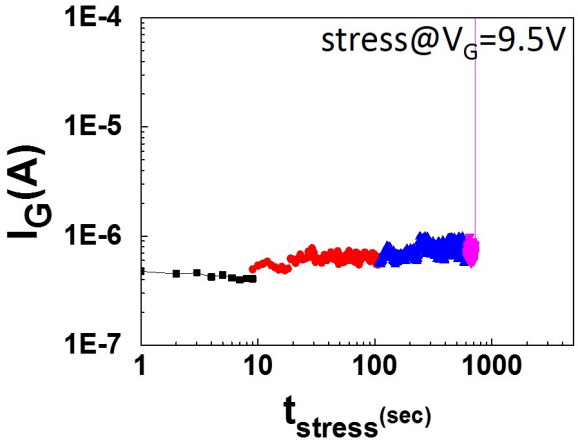

Figure 5.14: *Monitored I_G during the stress of V_G=9.5V.*

A further higher gate bias V_G=10V is stressed the device. A faster gate breakdown was observed, as shown in Figure 5.16. After a hard gate breakdown occurred, a serious I_D drop and a high leakage current are observed as well.

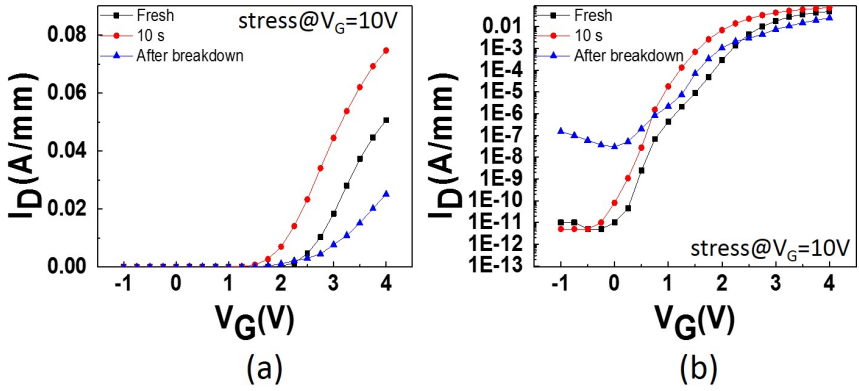

Figure 5.15: *I_D-V_G characteristics during the stress of V_G=10V in a linear-linear scale (a) and a logarithmic-linear scale (b).*

A faster time-dependent breakdown was observed under a stress of V_G=10V, as shown in Figure 5.16.

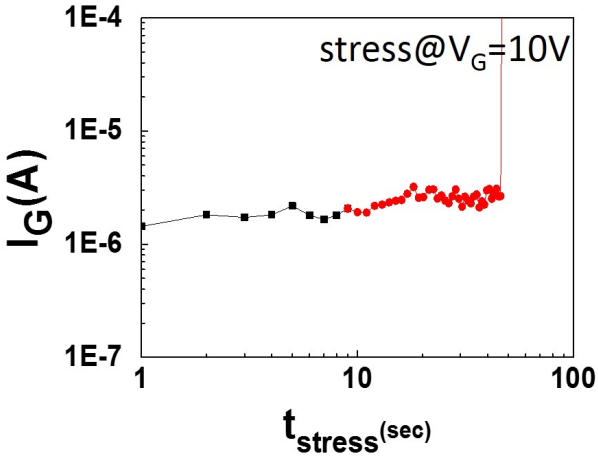

Figure 5.16: *Monitored I_G during the stress of V_G=10V.*

Figure 5.17 shows the summary of the monitored I_G under three different gate voltages, i.e. V_G=9V, V_G=9.5V, and V_G=10V. Time-dependent p-GaN HEMT under a high

forward gate voltage can be clearly observed. A high gate voltage results in a high gate leakage current, further leading to a early gate breakdown. Recent publications [139] [140] have observed the time-dependent behavior under a positive forward gate bias in a p-GaN HEMT as well.

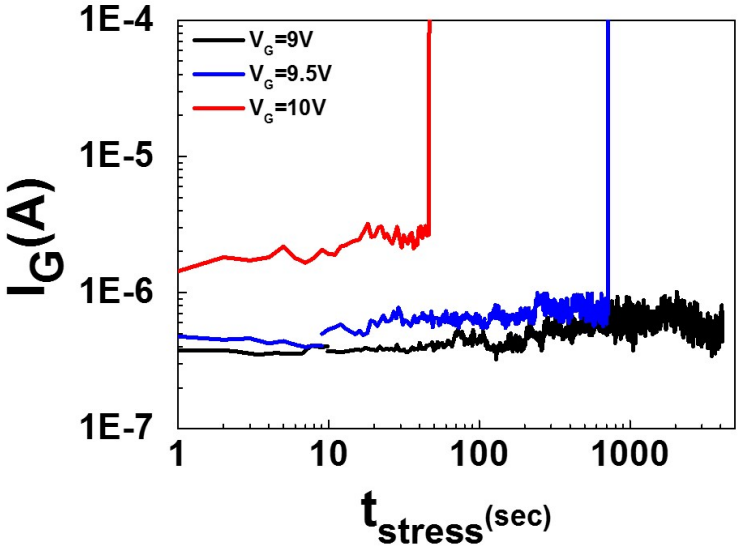

Figure 5.17: *Monitored I_G with three different gate voltages.*

The possible mechanisms leading to the time-dependent p-GaN gate breakdown could be due to the degradation in the p-GaN layer, where the region has a high electrical field. As shown in Figure 5.18, the holes in p-GaN gate could move under a positive gate bias. These holes could gradually damage and create the defects in the p-GaN layer, further forming a percolation path. Furthermore, the impact ionization, as mentioned previously, could further accelerate the degradation process in the p-GaN region since more and more electron-hole pairs are generated. Once the percolation path is formed, the p-GaN layer starts leaking and losing the capability to control the electrons in the channel. Therefore, a drop of I_D under a positive gate bias and an increase of the leakage current under a reversed gate bias are observed, as shown in Figure 5.13 and 5.15.

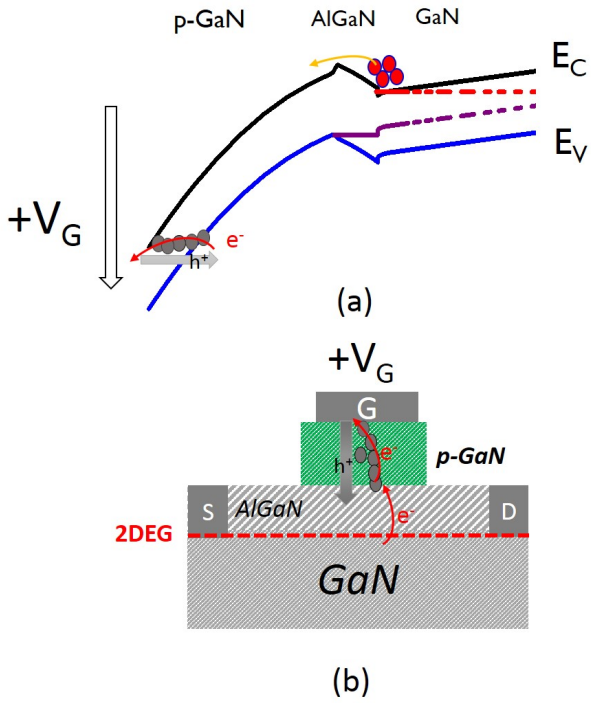

Figure 5.18: *Schematic of forming the percolation path under a positive gate bias.*

5.2.4 Conclusion of the high forward gate bias stress

In this section, preliminary high forward gate bias stresses are performed in p-GaN AlGaN/GaN HEMTs at room temperature. Generally, a negative V_{TH} shift was observed. When a higher gate bias is applied, a larger negative V_{TH} shift is observed. A possible reason could be due to hole movement and hole trapping by the interface states at the interface between p-GaN and AlGaN layer and by the bulk defects in the AlGaN layer.

Regarding the case of the stress at V_G=9V, there is no observable I_G degradation. However, when a higher gate bias is applied, e.g. V_G=9.5V and V_G=10V, a time-dependent p-GaN gate breakdown was observed. We have proposed that a percolation path is possibly formed in the p-GaN layer due to hole movement, resulting in a TDDB phenomenon.

5.3 Summary of this chapter

In this chapter, the forward bias gate breakdown mechanism and the stability under high forward gate stresses in Schottky metal/p-GaN gate AlGaN/GaN HEMTs have been studied. First of all, the positive temperature dependency of forward gate bias breakdown is observed. Such phenomenon can be explained by avalanche multiplication in the depletion region of the Schottky metal/p-GaN junction. Furthermore, the generation of electron-hole pairs under a high V_G bias is confirmed by an avalanche luminescence from EMMI measurement.

Secondly, under a forward gate bias stress at V_G=9V, a negative V_{TH} shift is observed. The possible mechanism related to the hole trapping has been proposed. The time-dependent p-GaN gate breakdown was observed during the stresses of V_G=9.5V, and V_G=10V. The formation of a percolation path in p-GaN region has been proposed to explain the TDDB behavior.

Chapter 6

Summary and outlook

This final chapter briefly reviews the main objective of this Ph.D. study, summarizes the Ph.D. work and the main contributions to the GaN scientific community, and finally gives an outlook of the future developments in GaN power devices.

6.1 Main Objective

GaN-on-Si power devices have shown superior performance with cost-effective solutions thanks to the large-diameter Si substrate and Au-free CMOS compatible processes. However, the long-term stability of GaN-on-Si power devices remains one of the serious bottlenecks for commercialization acceptance compared to the existing Si and SiC-based technologies. This Ph.D. study focuses on the evaluation of the stability of GaN-on-Si power devices under an ON-state condition, further analyzing the degradation mechanisms. These understandings can benefit the future improvement of the robustness of GaN power devices.

6.2 Summary of this Ph.D. work

In chapter 3, state-of-the-art D-mode AlGaN/GaN MIS-HEMTs with *in-situ* SiN/Al_2O_3 were first used to understand the stability under an ON-state stress although a D-mode MIS-HEMT is typically used in a normally-off cascode configuration, where the maximum gate bias is 0V. Two different instabilities have been identified: 1) Forward gate bias time-dependent dielectric breakdown, and 2) V_{TH} shift under a positive gate bias stress. Regarding the forward gate bias time-dependent dielectric breakdown, the TDDB methodology is demonstrated to evaluate the gate dielectric strength under a forward gate bias stress, showing an excellent dielectric strength at 200°C (a gate voltage of +5V or +6V for 1% of failures for 20 years lifetime). Secondly, V_{TH} stability under a forward gate bias stress is studied, indicating that a forward gate voltage (V_G)

bias stress induces a positive V_{TH} shift which is proportional to the applied gate forward voltage.

In chapter 4, three different instabilities in E-mode recessed gate GaN MIS-FETs have been investigated: 1) the impacts of the gate dielectric on the output drain current, 2) forward gate bias time-dependent dielectric breakdown, and 3) positive bias temperature instability (PBTI).

First of all, regarding the impacts of the gate dielectric on the output drain current, we found a reduction of output drain current when the gate dielectric interface is approaching the GaN channel due to a recessed gate approach. This is most probably due to scattering between the electrons in the channel and interface states/border traps when the gate dielectric approaches the GaN channel. This current reduction can be lowered by using a good quality gate dielectric, which has a lower D_{it} and border traps.

Secondly, a forward bias gate TDDB evaluation has been performed in D-mode MIS-HEMTs and E-mode MIS-FETs with a PEALD SiN gate dielectric (15nm and 25nm thickness). The conclusions are summarized in the following.

1) The β of the Weibull distribution with respect to the different recessed depth under the gate and different gate dielectric thickness has been discussed. We found that β becomes smaller for the device with a deeper recessed gate and the β becomes larger for the device with a thicker gate dielectric.

2) We have extracted the V_G with a criterion of 0.01% failures in the device with W_g=10μm after 20 years in MIS-HEMTs and MIS-FETs with different gate dielectric thickness. The extrapolated V_G is lower for a thinner AlGaN barrier under the gate. However, for MIS-FETs, the extrapolated V_G is larger for a deeper recessed gate.

3) Another percolation path around the gate corner could exist in a deeper recessed gate MIS-FET because the gate dielectric is thinner on the sidewall, as observed in the TEM inspection.

4) The Weibull distribution scaled with different W_g has been shown, indicating that the random generation of a percolation path along the direction of the W_g.

5) A maximum gate voltage of 4.9V (exponential law) or 7.2V (power law) is extrapolated with the criterion of 0.01% of failures for W_g=36mm at 150^{o}C after 20 years. This indicates that at least 25nm of a PE-ALD SiN gate dielectric is needed to have a sufficient TDDB margin with respect to this criterion. A slight improvement of the TDDB margin regarding this criterion is observed in the device with 25nm ALD Al_2O_3 gate dielectric.

Thirdly, PBTI in E-mode recessed gate MIS-FETs has been extensively characterized and discussed. The conclusions are summarized in the following.

1) The power law dependency of V_{TH} shift during a positive gate bias stress with respect to the stress time has been shown.

2) Regarding the time exponent (n), the voltage dependence of ΔV_{TH} (γ), and the activation energy (E_A), ALD Al_2O_3 gate dielectric shows a large n, γ, and E_A.

3) The defect band model is proposed to explain the different PBTI characteristics observed in the device with PEALD SiN and ALD Al_2O_3. Based on this model, the gate dielectric defects inside the PEALD SiN are much more easily accessible under a low gate voltage bias due to a wide defect band ($\sigma \sim 0.67$ eV) centered 0.05 eV below the conduction band (E_C - 0.05 eV) of GaN. On the other hand, the defect distribution inside the ALD Al_2O_3 is 1.15 eV away from the conduction band of GaN (E_C + 1.15 eV) and shows a narrower energy spread ($\sigma \sim 0.42$ eV). Therefore, the gate dielectric defect of ALD Al_2O_3 can only be accessed under a high gate voltage.

4) The overdrive voltage dependency of V_{TH} (γ) can correlate with the accessibility of dielectric defects in the gate dielectric. A low γ suggests the existence of a wide distribution of dielectric defects centered around the channel Fermi level, which can be easily accessed at low stress voltage. On the other hand, a high γ suggests a narrow distribution of defect levels far away from the channel Fermi level.

In chapter 5, the forward bias gate breakdown mechanism and the stability under high forward gate stresses in Schottky metal/p-GaN gate AlGaN/GaN HEMTs have been studied and discussed. The conclusions are summarized in the following.

1) A positive temperature dependency of the forward gate bias breakdown was observed. Such phenomenon is explained by avalanche multiplication in the depletion region of the Schottky metal/p-GaN junction since the electrons in the channel can be emitted over the AlGaN barrier and injected into the p-GaN, further being accelerated by the high electrical field.

2) Under forward gate bias stresses (V_G=9V, V_G=9.5V, and V_G=10V), a negative V_{TH} shift was observed, which is most probably due to hole movement and hole trapping by the interface states at the interface between p-GaN and AlGaN layer and by the bulk defects in the AlGaN layer.

3) A time-dependent p-GaN gate breakdown was observed during stress at V_G=9.5V and V_G=10V. This gate breakdown mechanism is attributed to a percolation path in the p-GaN region due to hole movement. After a hard breakdown, the drop of I_D and increase of the leakage current were observed.

6.3 Outlook

Regarding the ON-state instability identified and analyzed in this thesis, several aspects deserve further investigation. Among others, these are the most important ones:

The future work in MIS-HEMTs/MIS-FETs:

• Forward gate bias time-dependent dielectric breakdown (TDDB) has been successfully demonstrated in D-mode MIS-HEMTs and E-mode MIS-FETs at 150°C (chapter 4) and at 200°C (chapter 3). It could be interesting to understand the temperature acceleration of TDDB by performing TDDB as a function of the temperature.

• The model (Power law model or Exponential model) for lifetime extraction has to be verified for GaN-based devices although an appropriated model is still under debate even in Si-based technologies. This model is used to fit three data points, which needs a further validation. More stress voltage points in the TDB experiments especially toward lower stress voltage conditions can be included to verify the model.

• PBTI has been studied in the devices with two different gate dielectrics (PEALD SiN and Al_2O_3). Advanced gate dielectrics, such as HfO_2 or the bi-layer gate stack (SiO_x IL + HfO_2) is worth investigating the impacts on the PBTI since these gate dielectrics have been demonstrated in advanced logic devices to substantially improve PBTI, which can be explained by the reduction of the interface states density and the distribution of the gate dielectric defects. Therefore, these different gate dielectrics are also interesting to be further investigated in GaN-based devices.

The future work in p-GaN HEMTs:

• Although a positive temperature dependency of the gate breakdown has been shown in p-GaN HEMTs, the depletion region changes with respect to the different M_g concentration and a electric field might be different with respect to a different thickness of the p-GaN layer, leading to an impact on the forward gate breakdown mechanism. Investigation of forward gate breakdown mechanisms as a function of the M_g concentration and p-GaN layer thickness is needed and physical models with the impact of M_g concentration and p-GaN layer thickness should be discussed and included.

• Time-dependent p-GaN gate breakdown has been shown in this thesis. Further in-depth statistical studies regarding t_{BD} distributions are needed. It is necessary to know whether the t_{BD} distribution in p-GaN HEMTs follows the Weibull distribution or not. Furthermore, area scaling and lifetime calculation are also worth being performed.

• A possible mechanism to explain a negative V_{TH} shift under a high forward gate bias in p-GaN HEMTs was proposed, which is ascribed to hole trapping at the interface

between the p-GaN and the AlGaN layer. However, a systematic study is needed to verify this speculation. For example, different M_g concentration in the p-GaN layer and different thicknesses of the p-GaN layer might have impacts on hole trapping. These are worth studying to further consolidate this speculation.

• A possible mechanism to explain the TDDB in p-GaN HEMTs was proposed, which is most probably due to a percolation path in the p-GaN region. However, a systematic study is necessary to verify this speculation. For example, different p-GaN thicknesses might have a strong impact on the TDDB if the percolation path is formed in the p-GaN region. Therefore, future work including TDDB testing in p-GaN HEMTs with various p-GaN thickness is needed to verify the proposed mechanism.

In sum, future work to further investigate the ON-state reliability in enhancement mode GaN power devices has been proposed. This further work might not only dig out the degradation mechanisms but also stimulate the strategies to further improve the robustness of GaN power devices.

It is worth mentioning that not only ON-state but also SEMI-ON and OFF-state related reliability issues are needed to be explored in E-mode recessed gate MIS-FETs and p-GaN HEMTs. Furthermore, switching tests (hard switching and soft switching) might point out failure mechanisms which are not visible under constant DC stress conditions. All other stability issues, such as electromigration, ESD, high temperature storage, temperature cycling, radiation test, the stability of Ohmic contact, etc., have to be assessed, further identifying the failure mechanisms in GaN-based devices. These explorations can advance the understanding of the capability of GaN-based devices in power switching applications.

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Scientific Contributions and Awards

Honors and awards

• 2015 *IEEE Electron Device Letter* Golden Reviewer.

• 2014 *IEEE Electron Device Letter* Golden Reviewer.

• Fellowship for Long Stay Abroad Research, FWO, Belgium, 2015.

In the news

• "Forward-bias gate breakdown in HEMTs with enhancement-mode p-GaN gate" *Semiconductor Today*, 02. Sept. 2015.

International Journal Papers

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9. M. Meneghini, I. Rossetto, V. Rizzato, S. Stoffels, M. Van Hove, N. Posthuma, , **T.-L. Wu**, D. Marcon, S. Decoutere, G. Meneghesso, and E. Zanoni, "Gate Stability of GaN-Based HEMTs with P-Type Gate," *Electronics*, vol. 5, 2016.

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17. M. Meneghini, D. Bisi, D. Marcon, S. Stoffels, M. Van Hove, **T.-L. Wu**, S. Decoutere, G. Meneghesso, and E. Zanoni, "Trapping and Reliability assessment in d-mode GaN-based MIS-HEMTs for Power Applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2199-2207, May. 2014.

International Conference Proceedings

1. **T.-L. Wu**, J. Franco, D. Marcon, B. De Jaeger, M. Van Hove, B. Bakeroot, S. Stoffels, G. Groeseneken, and S. Decoutere, "Positive Bias Temperature Instability (PBTI) Evaluation in Fully Recessed Gate GaN MIS-FETs," in *Proc. IEEE International Reliability Physics Symposium (IRPS)*, pp. 4A.2.1-4A.2.6, 2016. (Pasadena, CA, USA, Apr. 17-21, 2016.)

2. **T.-L. Wu**, D. Marcon, B. De Jaeger, M. Van Hove, B. Bakeroot, D. Lin, S. Stoffels, X. Kang, R. Roelofs, G. Groeseneken, and S. Decoutere, "The impact of the gate dielectric quality in developing Au-free D-mode and E-mode recessed gate AlGaN/GaN transistors on a 200mm Si substrate," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 225-228, 2015. (Hong Kong, May. 10-14, 2015.)

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recessed gate D-mode and E-mode MIS-HEMTs," in *Proc. IEEE International Reliability Physics Symposium (IRPS)*, pp. 6C.4.1-6C.4.6, 2015. (Monterey, CA, USA, Apr. 19-23, 2015.)

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5. X. Kang, D. Wellekens, M. Van Hove, B. De Jaeger, N. Ronchi,**T.-L. Wu**, S. You, B. Bakeroot, J. Hu, X. Shi, D. Marcon, S. Stoffels, and S. Decoutere, "Device breakdown optimization of Al2O3/GaN MISFETs," in *Proc. IEEE International Reliability Physics Symposium (IRPS)*, pp. CD.5.1-CD.5.4, 2016. (Pasadena, CA, USA, Apr. 17-21, 2016.)

6. D. Marcon, M. Van Hove, D. Wellekens, N. Posthuma, S. You, X. Kang, **T.-L. Wu**, M. Willems, S. Stoffels and S. Decoutere, "Direct comparison of GaN-based e-mode architectures (recessed MISHEMT and p-GaN HEMTs) processed on 200mm GaN-on-Si with Au-free technology," in *Proc. SPIE, Gallium Nitride Materials and Devices X*, 936311, 2015. (San Francisco, CA, USA, Feb. 07-12, 2015.)

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International Conference Abstracts

1. **T.-L. Wu**, D. Marcon, B. De Jaeger, N. Posthuma, B. Bakeroot, S. You, J. Franco, S. Stoffels, M. Van Hove, G. Groeseneken, and S. Decoutere, "Gate stability of enhancement mode GaN power devices," *12th INC global nanotechnology conference*, Leuven, Belgium, 10-12 May, 2016.

2. **T.-L. Wu**, D. Marcon, S. Stoffels, S. You, B. De Jaeger, M. Van Hove, G. Groeseneken, and S. Decoutere, "Stability evaluation of Au-free Ohmic contacts on AlGaN/GaN HEMTs under a constant current stress," *25th European Symposium On Reliability Of Electron Devices, Failure Physics and Analysis (ESREF)*, Berlin, Germany, 29. Sept-02. Oct., 2014.

3. **T.-L. Wu**, D. Marcon, M. Zahid, M. Van Hove, S. Stoffels, P. Srivastava, S. Decoutere, and G. Groeseneken, "Forward Gate Bias On-State Stress on

AlGaN/GaN MIS-HEMTS for Power Switching Applications," *36th Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE)*, Island of Porquerolles, France, 28-30 May, 2012.

4. G. Meneghesso, M. Meneghini, I. Rossetto, V. Rizzato, S. Stoffels, M. Van Hove, **T.-L. Wu**, S. You, N. Posthuma, S. Decoutere, and E. Zanoni, "Normally-off HEMTs with p-GaN Gate: Stability and Lifetime Extrapolation," *International Workshop on Nitride Semiconductors (IWN)*, 2016. (submitted)

5. I. Rossetto, M. Meneghini, V. Rizzato, S. Stoffels, M. Van Hove, N. Posthuma, **T.-L. Wu**, D. Marcon, S. Decoutere, G. Meneghesso and E. Zanoni, "Study of the stability of e-mode GaN HEMTs with p-GaN gate based on combined DC and optical analysis," *27th European Symposium On Reliability Of Electron Devices, Failure Physics and Analysis (ESREF)*, Halle (Saale), Germany, 19-22 Sept., 2016.

6. I. Rossetto, M. Meneghini, D. Bisi, M. Van Hove, D. Marcon, **T.-L. Wu**, B. De Jaeger, S. Decoutere, G. Meneghesso, E. Zanoni, "Impact of gate insulator on the dc and dynamic performance of AlGaN/GaN MIS-HEMTs," *26th European Symposium On Reliability Of Electron Devices, Failure Physics and Analysis (ESREF)*, Toulouse, France, 05-09 Oct. 2015.

7. D. Marcon, M. Van Hove, B. De Jaeger, D. Wellekens, N. Posthuma, S. You, B. Bakeroot, X. Kang, **T.-L. Wu**, M. Willems, S. Stoffels and S. Decoutere, "200mm GaN-on-Si Status : Comparison of e-Mode p-GaN and Recessed MISHEMT Devices," *Asia-Pacific Microwave Conference (APMC)*, Sendai, Japan, 04-07 Nov., 2014.

8. N. Ronchi, B. De Jaeger, M. Van Hove, R. Roelofs, **T.-L. Wu**, J. Hu, X. Kang, and S. Decoutere. "Combined PEALD gate-dielectric and in-situ SiN cap-layer for reduced Vth shift and RDS-ON dispersion of AlGaN/GaN HEMTs on 200 mm Si wafer," *46th International Conference on Solid State Devices and Materials (SSDM)*, Tsukuba, Japan, 8-11 Sept., 2014.

9. J. Hu, S. Stoffels, S. Lenci, **T.-L. Wu**, N. Ronchi, S. You, B. Bakeroot, G. Groeseneken, and S. Decoutere, "Study of Constant Voltage Off-state Stress on Au-free AlGaN/GaN Schottky Barrier Diodes," *46th International Conference on Solid State Devices and Materials (SSDM)*, Tsukuba, Japan, 8-11 Sept., 2014.

10. M. Meneghini, D. Bisi, D. Marcon, M. Van Hove, **T.-L. Wu**, S. Decoutere, G. Meneghesso, and E. Zanoni, "Investigation of the impact of hot electrons and high drain bias on the dynamic Ron increase in GaN-based MIS-HEMTs grown on silicon,"*International Workshop on Nitride Semiconductors (IWN)*, Wroclaw, Poland, 24-19 Aug., 2014.

11. M. Meneghini, D. Bisi, D. Marcon, S. Stoffels, M. Van Hove, **T.-L. Wu**, S. Decoutere, G. Meneghesso, and E. Zanoni, "Ron collapse, breakdown and degradation of d-mode MIS-HEMTs based on GaN on Si technology," *10th International Conference on Nitride Semiconductors (ICNS)*, Washington DC, USA, 25-30 Aug., 2013.

12. M. Zahid, D. Marcon, M. Van Hove, **T.-L. Wu**, and S. Decoutere, "Lifetime investigation of Si3N4/Al2O3 as gate dielectric for AlGaN/GaN MIS-HEMTs studied with Time Dependent Dielectric Breakdown," *36th Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE)*, Island of Porquerolles, France, 28-30 May, 2012.

Invited Seminars

1. **T.-L. Wu**, "AlGaN/GaN-based transistors for power switching applications and their reliability issues," Department of Electrical Engineering, National Central University (NCU), Tayouan, Taiwan, Mar. 2016.

2. **T.-L. Wu**, "Interface characterizations and PBTI in GaN power devices," IBM research, Albany, USA, Jan. 2016.

3. **T.-L. Wu**, "AlGaN/GaN-based transistors for power switching applications and their reliability issues," Department of Electronics Engineering, National Chiao Tung University (NCTU), Hsinchu, Taiwan, Dec. 2015.

4. **T.-L. Wu**, "Reliability issues in GaN HEMTs," Reliability workshop, imec, Leuven, Belgium, Sept. 2015. (Joint presentation with Dr. D. Marcon.)

5. **T.-L. Wu**, "AlGaN/GaN-based transistors for power switching applications and their reliability issues," Department of Engineering and System Science, National Tsing Hua University (NTHU), Hsinchu, Taiwan, Dec. 2014.

Curriculum Vitae

吳添立 Tian-Li Wu was born in Zhongli District, Taoyuan City, Taiwan. He received the B.S. degree in Electrical Engineering from National Chung Hsing University (NCHU), Taichung, Taiwan, in 2006 and received the M.S. degree in Electronics Engineering from National Tsing Hua University (NTHU), Hsinchu, Taiwan, in 2008, where he focused on the development of SiC-based devices for RF and high voltage applications. Since Sept. 2011, he works in the GaN power device group, led by Dr. Stefaan Decoutere, at imec, Leuven, Belgium. Since June 2012, he becomes a Ph.D. candidate in the Department of Electrical Engineering, University of Leuven (KU Leuven), Belgium, under the guidance of Prof. Guido Groeseneken and Dr. Denis Marcon. His research interests focus on the development of GaN technology for power switching applications and the investigation of reliability issues in GaN power devices.

From Feb. 2013 till June 2015, he worked as a teaching assistant at KU Leuven for the course "Reliability and Yield for Micro- and Nanoelectronic Components" (Instructor: Prof. Guido Groeseneken). From Jan. 2016 till Mar. 2016, he visited the FEOL/MOL reliability research group, led by Dr. James Stathis, in IBM research, NY, USA, where he focused on interface characterization in sub-10nm SiGe pMOS FinFETs.

By the end of the Ph.D. study, he has authored/co-authored with 35+ technical paper and has participated in the several international conferences to present his research, including IRPS in 2016, 2015, and 2013, ISPSD in 2015, ESREF in 2014, and WOCSDICE in 2012.

He is a reviewer for *IEEE Electron Device Letters* (2014 and 2015 Golden Reviewer) and *IEEE Transactions on Electron Devices*. He served as the President and Supervisor of the Taiwanese student association in Leuven (TSAL), Belgium, from July 2012 till June 2014.

FACULTY OF ENGINEERING SCIENCE
DEPARTMENT OF ELECTRICAL ENGINEERING
imec, Kapeldreef 75
B-3001 Heverlee, Belgium
Tian-Li.Wu@imec.be
http://www.esat.kuleuven.be